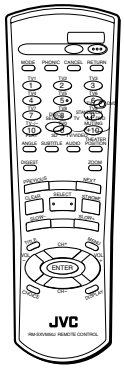
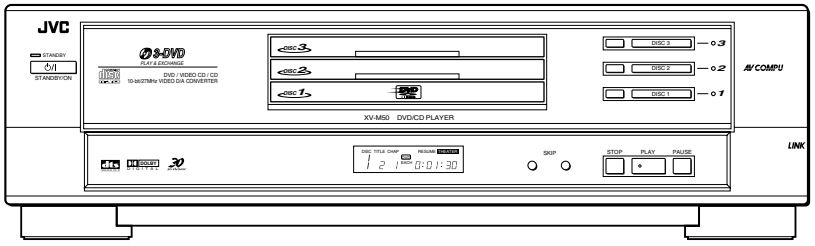
JVC

SERVICE MANUAL

DVD VIDEO PLAYER

XV-M52SL
XV-M50BK





[XV-M52SL]

Area Suffix

B ---------- U.K.
EN ----- Northern Europe
UN ---------- Asean
US ---------- Singapore
UW -- Brazil,Mexico,Peru

[XV-M50BK]

Area Suffix

UJ ---------- U.S.military

Each difference point

Model	Body color
XV-M50BK	Black
XV-M52SL	Silver

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▬) and ICP (⬬) or identified by the "⚠" mark nearby are critical for safety.
When replacing them, be sure to use the parts of the same type and rating as specified by the manufacturer. (Except the JC version)

Contents

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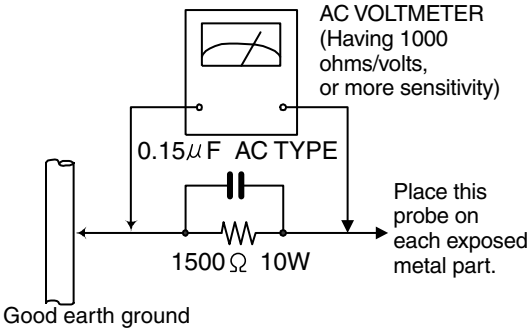
No.A0015
July, 2001

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet, particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.).
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
     Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to eachexposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. Voltage measured any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ CAUTION

Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.

In regard with component parts appearing on the silk-screen printed side (parts side) of the PWB diagrams, the parts that are printed over with black such as the resistor (▬), diode (▮) and ICP (●) or identified by the "⚠" mark nearby are critical for safety.
When replacing them, be sure to use the parts of the same type and rating as specified by the manufacturer. (Except the J and C version)

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.1. Grounding to prevent damage by static electricity

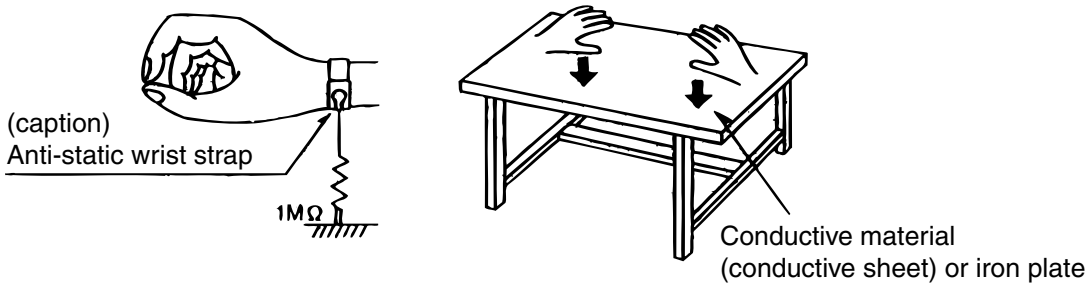
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the next page.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. For specific details, refer to the replacement procedure in the text. Be careful not to take too long a time when attaching it to the connector.

3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Precautions for Service

Handling of Traverse Unit and Laser Pickup

1. Do not touch any peripheral element of the pickup or the actuator.
2. The traverse unit and the pickup are precision devices and therefore must not be subjected to strong shock.
3. Do not use a tester to examine the laser diode. (The diode can easily be destroyed by the internal power supply of the tester.)
4. When replacing the pickup, after mounting a new pickup, remove the solder on the short land which is provided at the center of the flexible wire to open the circuit.
5. Half-fixed resistors for laser power adjustment are adjusted in pairs at shipment to match the characteristics of the optical block.
   Do not change the setting of these half-fixed resistors for laser power adjustment.

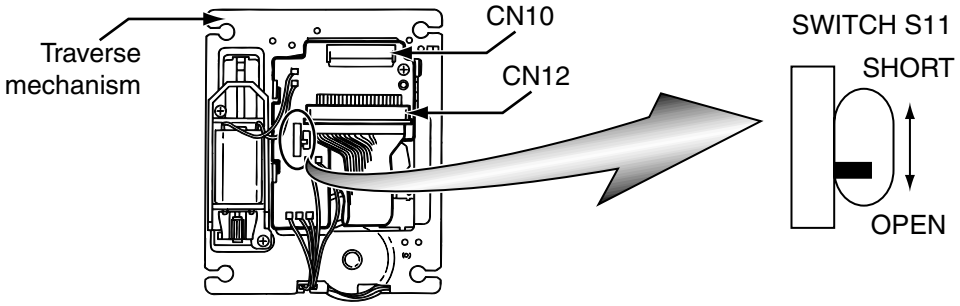
Destruction of Traverse Unit and Laser Pickup by Static Electricity

Laser diodes are easily destroyed by static electricity charged on clothing or the human body. Before repairing peripheral elements of the traverse unit or pickup, be sure to take the following electrostatic protection:

1. Wear an antistatic wrist wrap.
2. With a conductive sheet or a steel plate on the workbench on which the traverse unit or the pick up is to be repaired, ground the sheet or the plate.

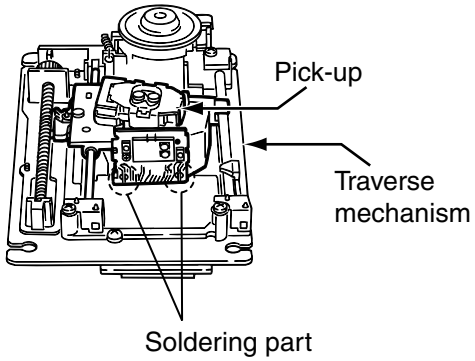
When you remove the traverse mechanism from the servo control substrate

The laser diode of pick-up might be destroyed by static electricity and set switch (S11) on the pick-up board on "SHORT" side, please before removing the card wire from connector (CN10).
Moreover, please set switch (S11) on "OPEN" side after assembling and inserting the card wire in connector (CN10) without fail at times.



When you remove the pick-up from the traverse mechanism

The laser diode of the pick-up might be destroyed by static electricity, and solder with part a, please before extracting a flexible wire from connector (CN12).
Moreover, please remove solder in part a after inserting a flexible wire in connector (CN12).



Disassembly method

<Main body>

■ Removing the top cover (See Fig.1)

1. Remove the two screws **A** attaching the top cover on the back of the body.

2. Remove the four screws **B** attaching the top cover on both sides of the body.

3. Pull the lower parts of the top cover sides and remove the top cover in the direction of the arrow.

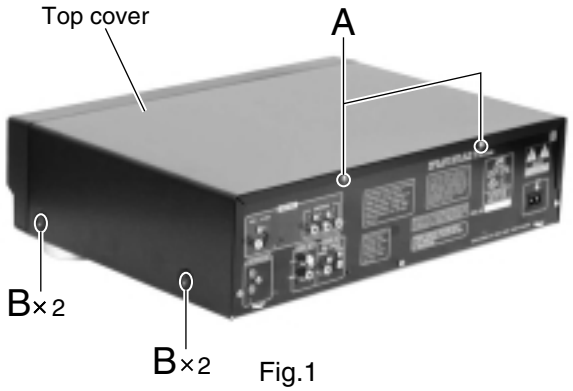


Fig.1

■ Removing the front panel assembly (See Fig.2 to 5)

・ Prior to performing the following procedure, remove the top cover.

1. Disconnect the wire from connector CN971 on the power supply board.

2. Disconnect the card wire from connector CN703 on the system control board.

3. Remove the three screws **C** attaching the front panel assembly on the bottom of the body.

4. Release the joint **a** on the bottom and the two joints **b** on both sides of the body. Remove the front panel assembly toward the front.

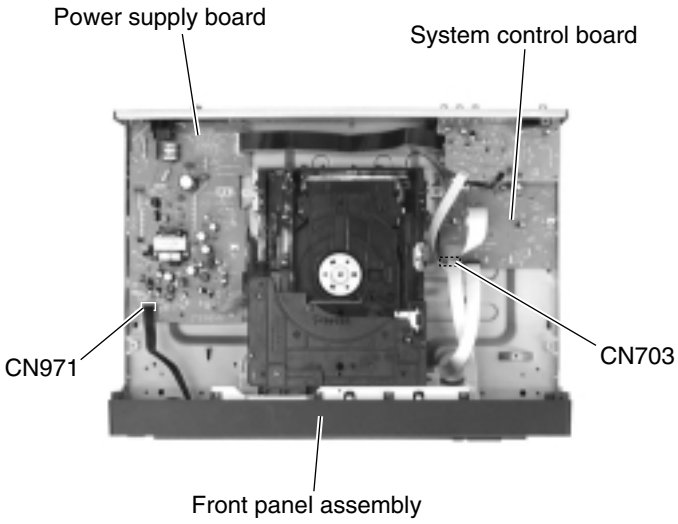


Fig.2

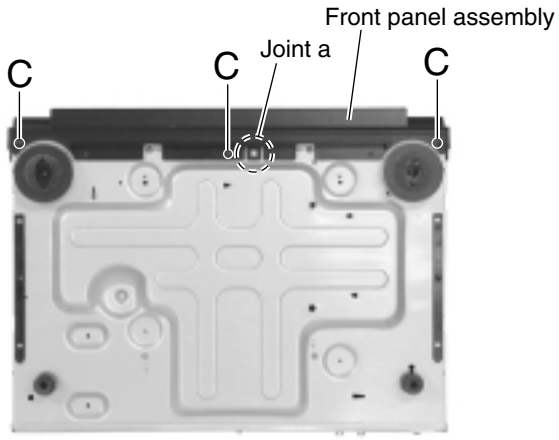


Fig.3

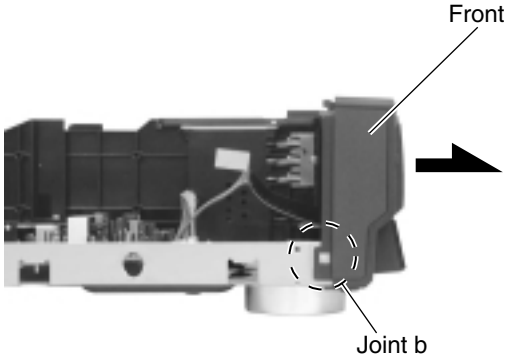


Fig.4

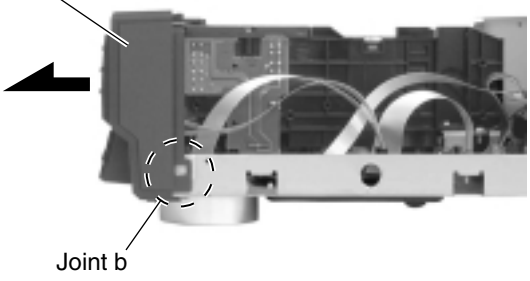


Fig.5

■ Removing the rear panel (See Fig.6)

・ Prior to performing the following procedure, remove the top cover.

1. Remove the eleven screws **D** attaching the rear panel on the back of the body and detach the rear panel.

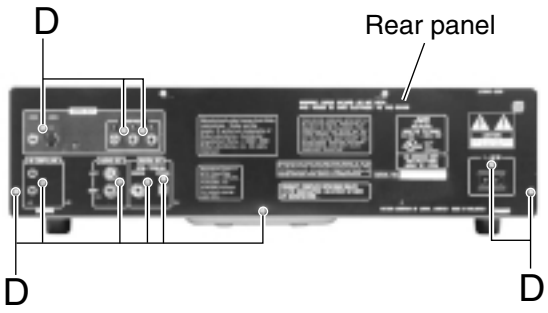


Fig.6

■ Removing the DVD changer mechanism assembly (See Fig.7)

・ Prior to performing the following procedure, remove the top cover and front panel assembly.

1. Remove the one screw **E**.
2. Disconnect the 9 pin wire from connector CN961 on the power supply board.
3. Disconnect the card wire from connector CN601 on the video board.
4. Disconnect the card wires from connector CN701 and CN702 on the system control board.
5. Remove the four screws **F** attaching the DVD changer mechanism assembly.

・ It is easy for removing the front panel assembly to remove the mechanism assembly though the mechanism assembly can be removed even in the state that the front panel assembly adheres.

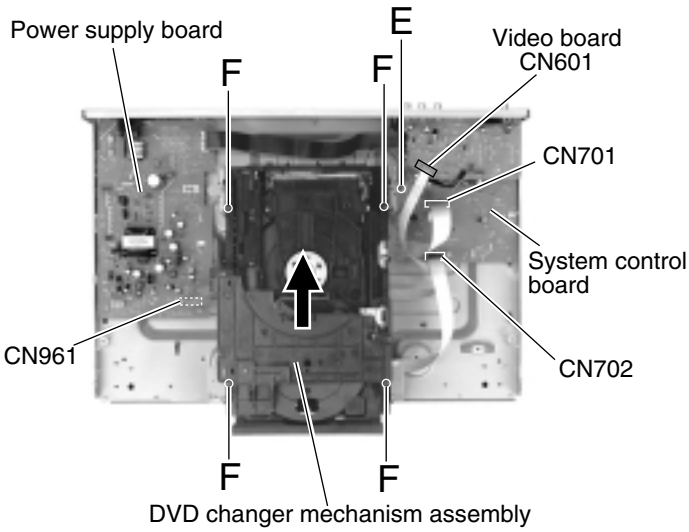


Fig.7

■ Removing the power supply board (See Fig.8 and 9)

・ Prior to performing the following procedure, remove the top cover.

1. Disconnect the wire from connector CN971 on the power supply board (The wire is extending from the front panel assembly).

2. Disconnect the 9 pin wire from connector CN961 on the power supply board (The wire is extending from the DVD changer mechanism assembly).

3. Disconnect the wire from connector CN951 and CN952 on the power supply board (The wire is extending from the system control board).

4. Remove the screw **D** attaching the AC jack on the rear panel.

5. Remove the two screws **G** attaching the power supply board and detach the power supply board.

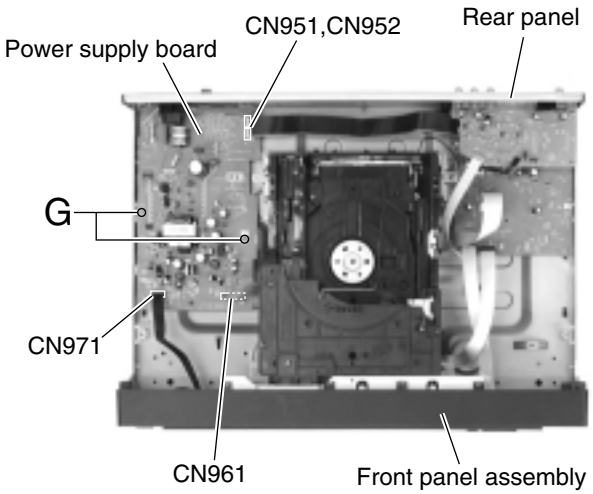


Fig.8

Fig.9

■ Removing the video board (See Fig.10 and 11)

- Prior to performing the following procedure, remove the top cover.

1. Disconnect the card wire from connector CN601 on the video board (The card wire is extending from the DVD changer mechanism assembly).

2. Disconnect the wire from connector CN704 on the system control board (The wire is extending from the video board).

3. Remove the three screws **D** attaching the video board on the rear panel. Pull out the video board from the rear panel.

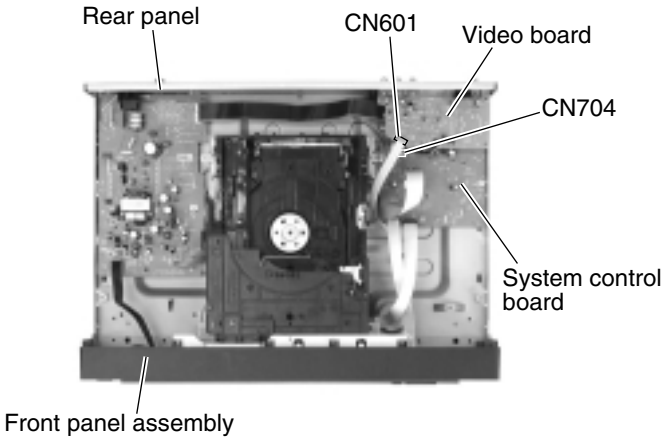


Fig.10

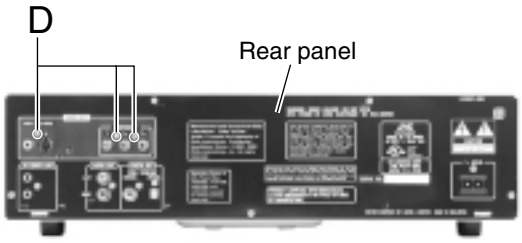


Fig.11

■ Removing the system control board (See Fig.12 and 13)

- Prior to performing the following procedure, remove the top cover.
- The system control board can be removed even if the video board is attached.

1. Disconnect the card wire from connector CN703 on the system control board (The card wire is extending from the front panel assembly).

2. Disconnect the card wire from connector CN701 and CN702 on the audio board (The card wires are extending from the DVD changer mechanism assembly).

3. Disconnect the wire from connector CN704 on the system control board (The wire is extending from the video board).

4. Disconnect the wire from connector CN951 and CN952 on the power supply board (The wire is extending from the system control board).

5. Remove the screw **H** attaching the system control board.

6. Remove the four screws **D** attaching the system control board on the rear panel. Pull out the system control board toward the front.

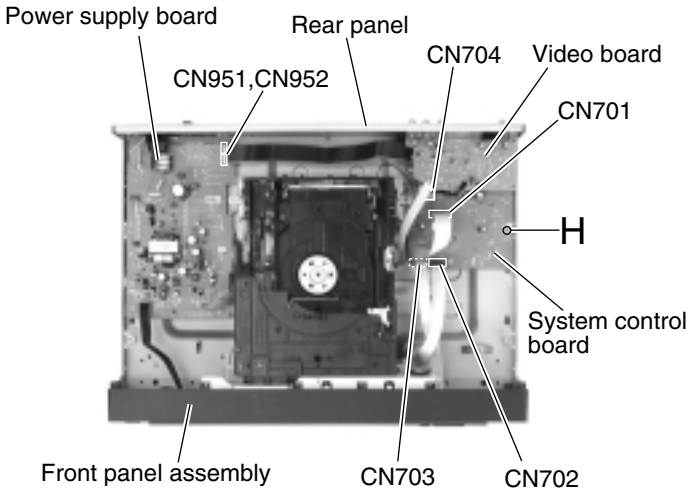


Fig.12

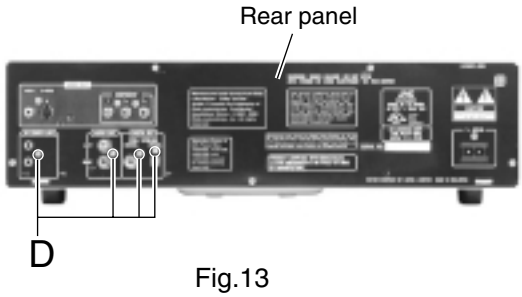


Fig.13

<Front panel assembly>

・Prior to performing the following procedure, remove the top cover and the front panel assembly.

■Removing the front board (See Fig.14 and 15)

1. Remove the two screws **I** on the back of the front panel assembly and remove the bracket from the front panel assembly.

2. Remove the seven screws **J** attaching the front board.

   If necessary, unsolder FW803 and disconnect the wire.

■Removing the STANDBY switch board (See Fig.16)

1. Remove the two screws **K** on the back of the front panel assembly.

   If necessary, unsolder FW803 and disconnect the wire.

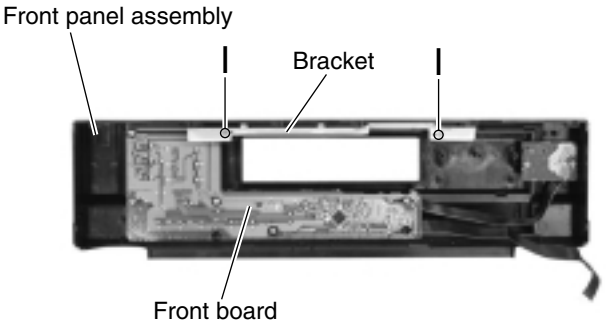


Fig.14

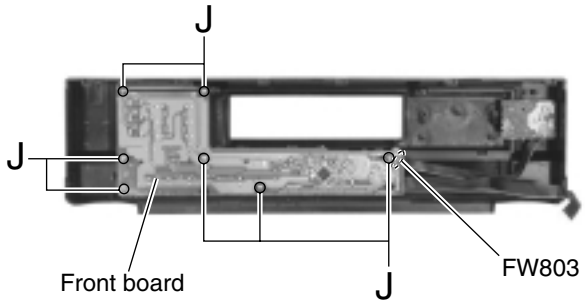


Fig.15

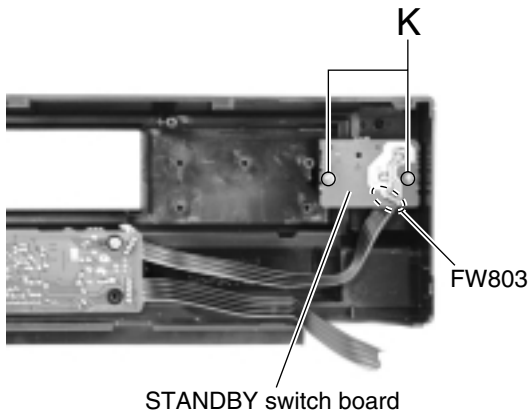


Fig.16

<DVD changer mechanism assembly>

・Prior to performing the following procedure, remove the top cover and the DVD changer mechanism assembly.

■Removing the traverse mechanism control board (See Fig.17)

1. Disconnect the card wire from connector CN101 on the traverse mechanism control board on the bottom of the DVD changer mechanism assembly.

2. Remove the screw L attaching the traverse mechanism control board. Release the three parts e, f and g and remove the traverse mechanism control board.

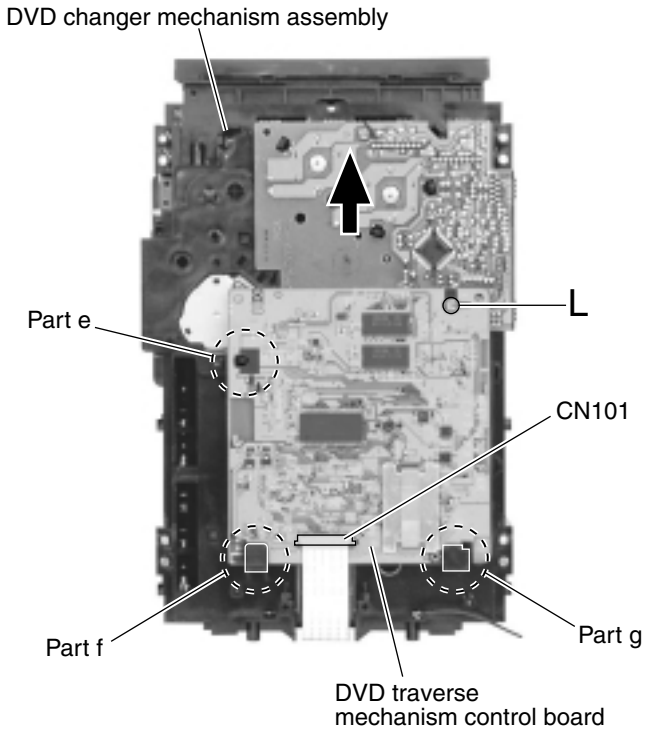


Fig.17

Ejecting the DVD (See Fig.18 and 19)

■When the DVD is set or the traverse mechanism is up.

※The DVD tray can not be ejected when the traverse mechanism is up.

■Bringing down the traverse mechanism as shown in the Fig.20

1. The motor pulley and the belt can be seen on the front side of the changer. Turn the motor pulley clockwise until the belt stops.

2. Pull the tray lock lever on the left side of the changer and draw the DVD tray.

3. Draw the DVD tray 1 to 3 as above.

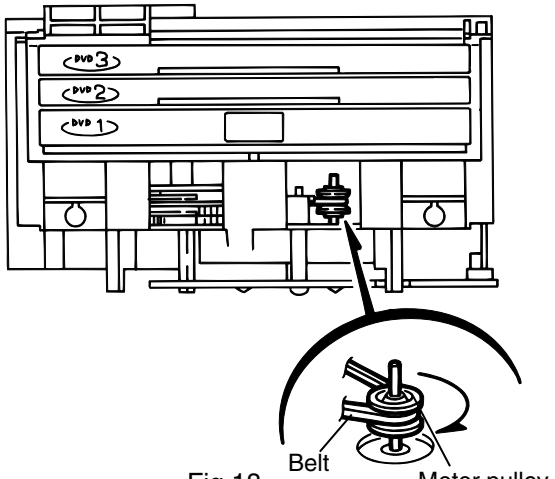


Fig.18

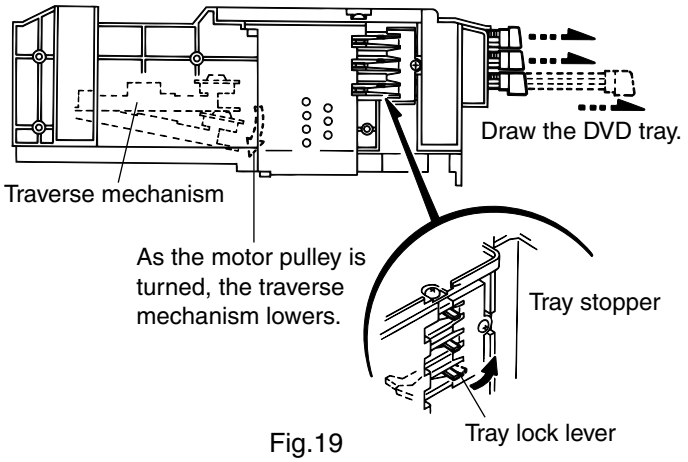


Fig.19

<DVD Changer Mechanism Section>

■Removing the DVD mechanism board (See Fig.1)

1. Remove the DVD changer mechanism assembly.
2. From bottom side the DVD changer mechanism assembly, remove the one screw **A** retaining the DVD servo control board.
3. Disconnect the card wire from the connector CN101 on the DVD servo control board.
4. Disengage the one engagement **a** and two engagements **b** , remove the DVD servo control board.

ATTENTION !

The laser diode of pick-up might be destroyed by static electricity and set switch (S11) on the pick-up board on "SHORT" side, please before removing the card wire from connector (CN101).
Moreover, please set switch (S11) on "OPEN" side after assembling and inserting the card wire in connector (CN101) without fail at times.

Please refer to page 1-4 for a detailed content.

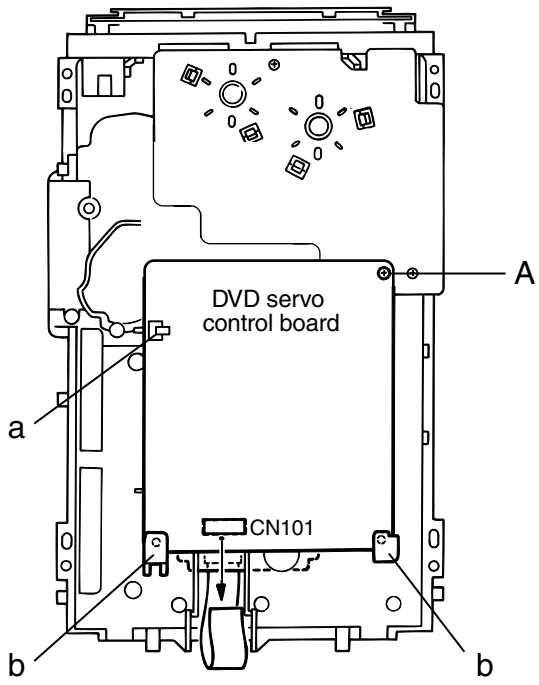


Fig.1

■Removing the DVD tray assembly (See Fig.2~4)

1. Remove the screw **B** retaining the Disc stopper (See Fig.3).
2. Remove the three screws **C** retaining the T.bracket (See Fig.3).
3. From the clamper base section **c**, remove both of the edges fixing the rod(See Fig.2 and 3).
4. Remove the screw **D** retaining the clamper assembly (See Fig.3).
5. From the left side face of the chassis assembly, remove the one screw **E** retaining both of the return spring and lock lever(See Fig. 4).
6. By removing the pawl at the section **d** fixing the return spring, dismount the return spring(See Fig.4).
7. Remove the three lock levers(See Fig.4).

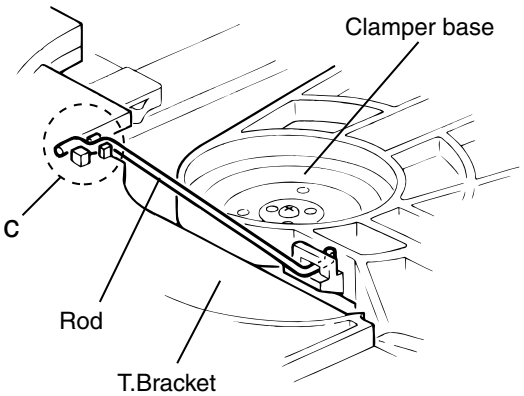


Fig.2

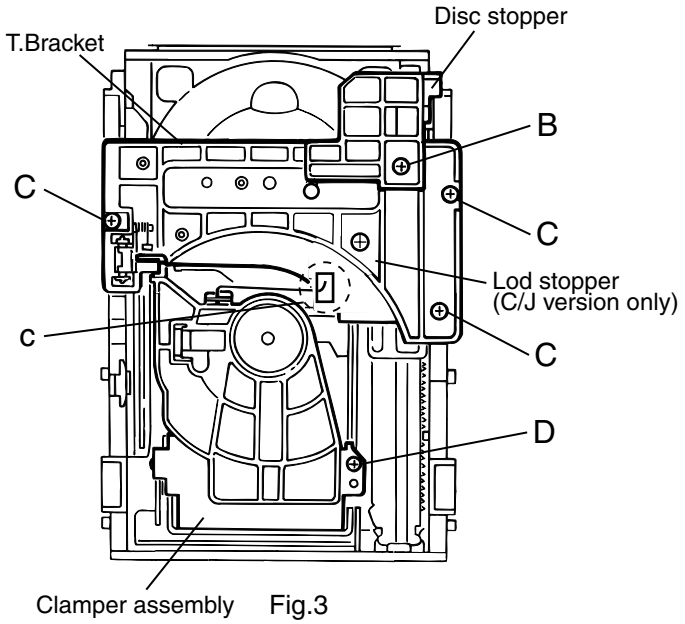


Fig.3

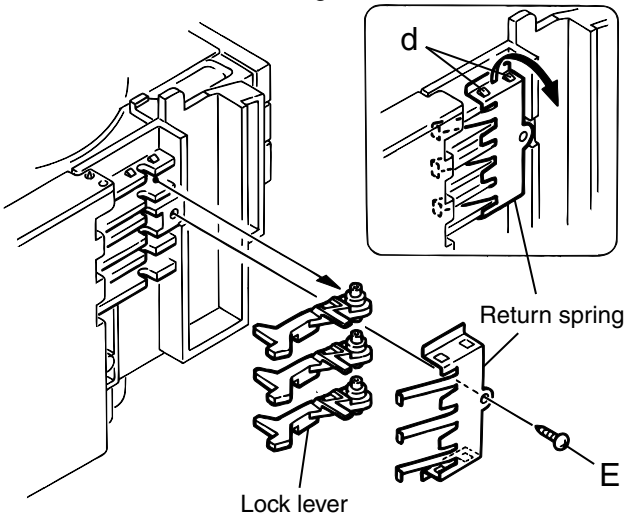


Fig.4

8. Check whether the lifter unit stopper has been caught into the hole at the section **e** of DVD tray assembly as shown in Fig.5.
9. Make sure that the driver unit elevator is positioned as shown in Fig.6 from to the second or fifth hole on the left side face of the DVD Traverse mechanism assembly.

[Caution] In case the driver unit elevator is not at above position, set the elevator to the position as shown in Fig.7 by manually turning the pulley gear as shown in Fig.8.

10. Manually turn the motor pulley in the clockwise direction until the lifter unit stopper is lowered from the section **e** of DVD tray assembly(See Fig.8).
11. Pull out all of the three stages of DVD tray assembly in the arrow direction **f** until these stages stop (See Fig.6).
12. At the position where the DVD tray assembly has stopped, pull out the DVD tray assembly while pressing the two pawls **g** and **g'** on the back side of DVD tray assembly(See Fig.9). In this case, it is easy to pull out the assembly when it is pulled out first from the stage DVD tray assembly.

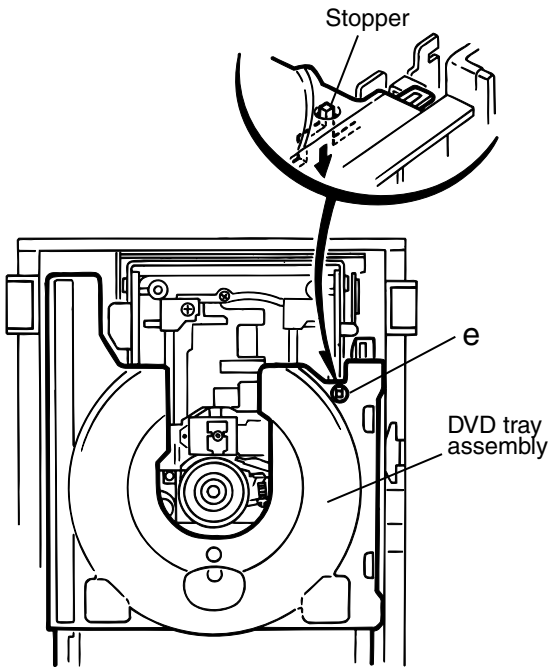


Fig.5

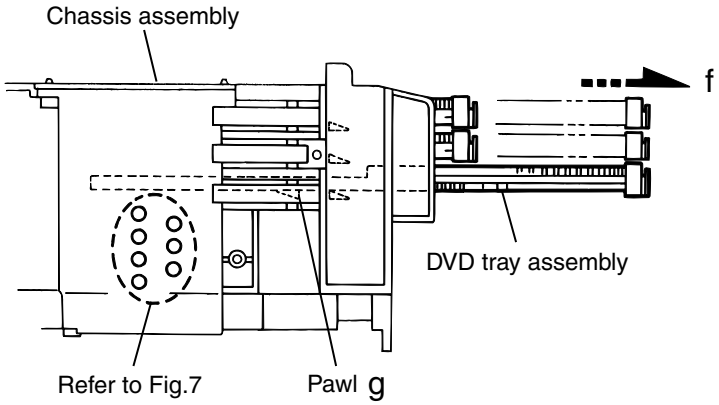


Fig.6

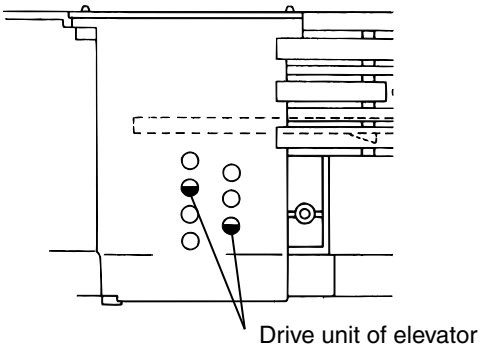


Fig.7

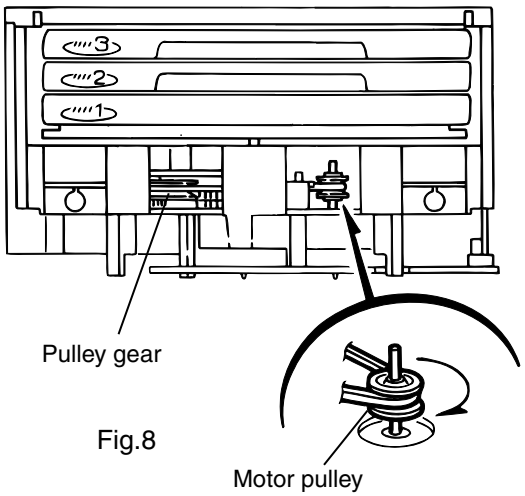


Fig.8

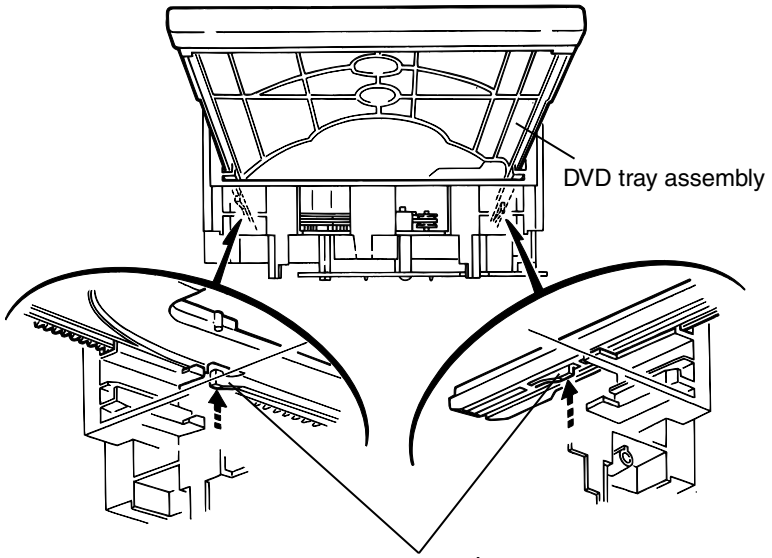


Fig.9

■ Removing the DVD mechanism assembly(See Fig.10)

1. While turning the cams R1 and R2 assembly in the arrow direction **h** , align the shaft **i** of the DVD mechanism assembly to the position shown in Fig.10.
2. Remove the four screw **F** retaining the DVD mechanism assembly.

■ Removing the DVD traverse mechanism assembly (See Fig.11 and 12)

1. For dismounting only the DVD mechanism without removing the DVD mechanism assembly, align the shaft **j** of the DVD mechanism assembly to the position shown Fig.11 while turning the cam R1 and R2 assembly in the arrow direction **k**.
2. Remove the two screws **G** raising the DVD mechanism assembly.
3. Remove the DVD traverse mechanism assembly in the arrow direction **l** from the lifter unit (See Fig. 12)

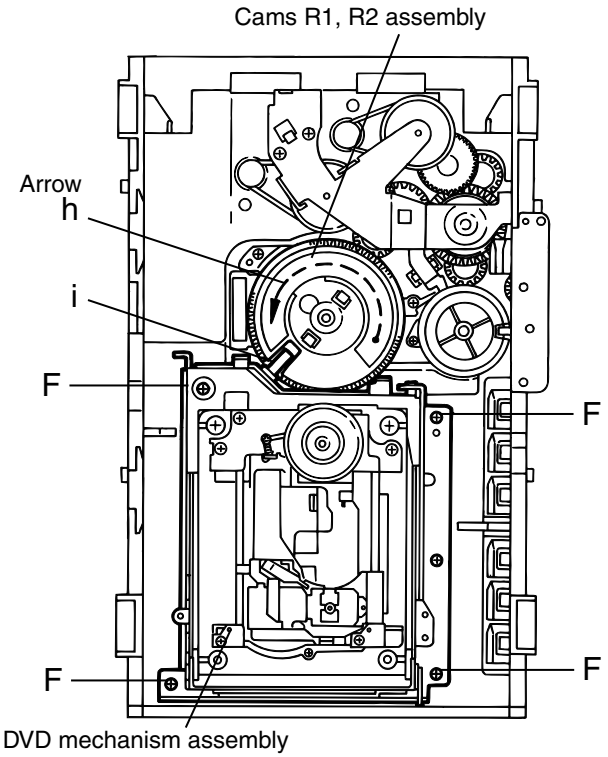


Fig.10

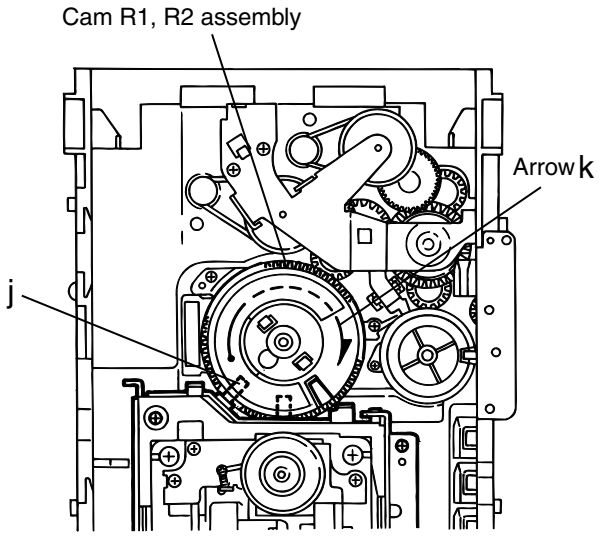


Fig.11

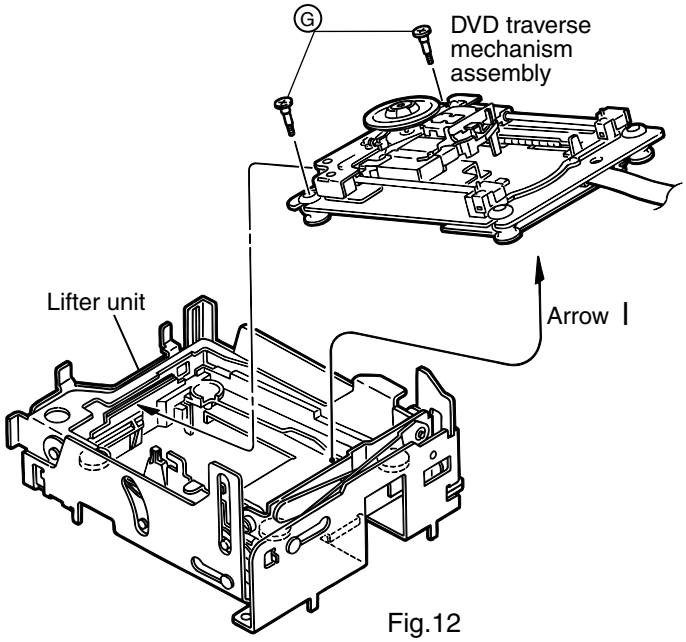


Fig.12

■ Removing the mechanism control board (See Fig.14, 15)

1. Absorb the four soldered positions **m** of the right and left motors with a soldering absorber(See Fig.14).
2. Remove the two screws **H** retaining the mechanism control board(See Fig.14).
3. Remove the two screws **I** retaining the tray select switch board(See Fig.15).

■ Removing the cam unit (See Fig.15 ~ 18)

1. Remove the DVD mechanism assembly.
2. While turning the cam gear **L**, align the pawl **n** position of the drive unit to the notch position(Fig.15) on the cam gear **L**.
3. Pull out the drive unit and cylinder gear(See Fig.17).
4. While turning the cam gear **L**, align the pawl **o** position of the select lever to the notch position(Fig.18) on the cam gear **L**.
5. Remove the four screws **J** retaining the cam unit(cam gear **L** and cams R1/R2 assembly)(See Fig.18).

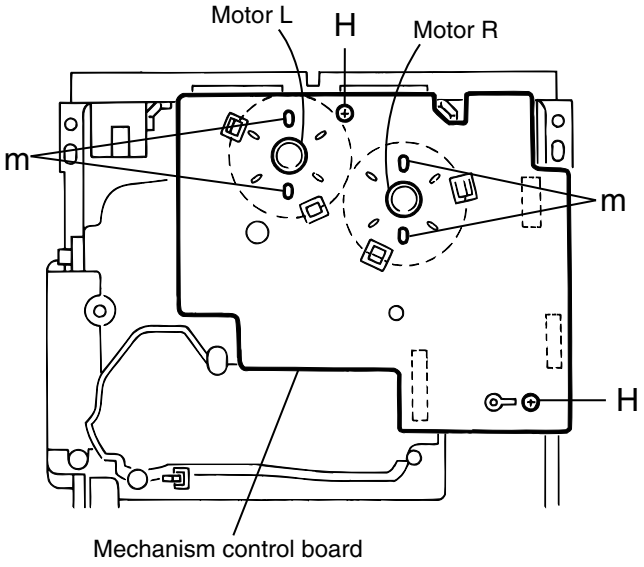


Fig.14

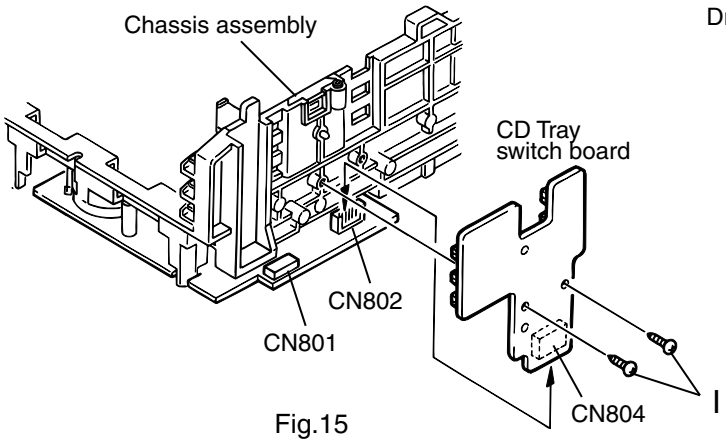


Fig.15

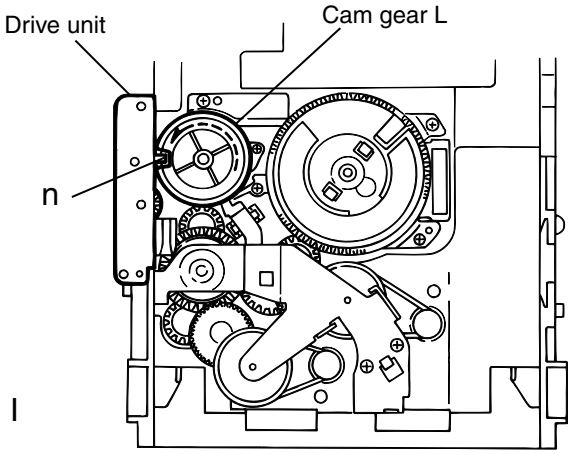


Fig.16

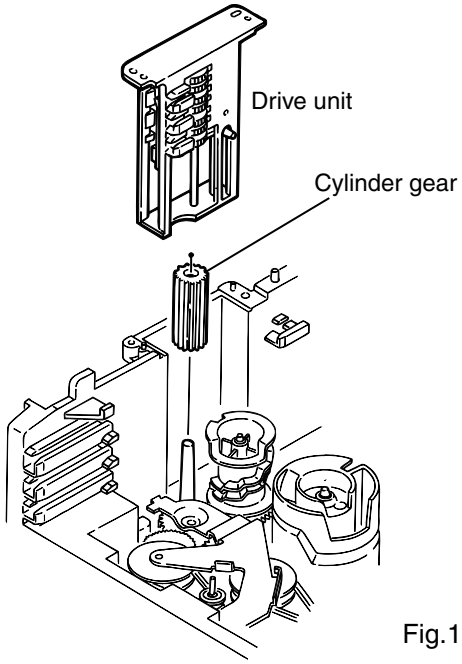


Fig.17

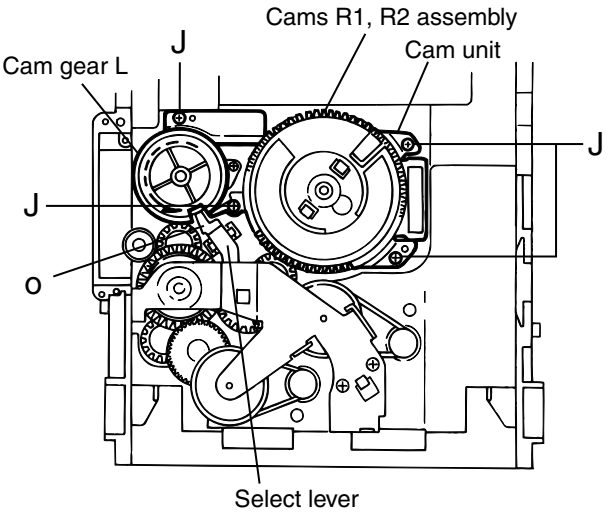


Fig.18

■ Removing the actuator motor and belt (See Fig.19～22)

1. Remove the two screws **K** retaining the gear bracket (See Fig.19).
2. While pressing the pawl **p** fixing the gear bracket in the arrow direction, remove the gear bracket (See Fig.19).
3. From the notch **q** section on the chassis assembly fixing the edge of gear bracket, remove and take out the gear bracket(See Fig. 20).
4. Remove the belts respectively from the right and left actuator motor pulleys and pulley gears(See Fig. 19).
5. After turning over the chassis assembly, remove the actuator motor while spreading the four pawls **r** fixing the right and left actuator motors in the arrow direction(See Fig. 21).

[Note] When the chassis assembly is turned over under the conditions wherein the gear bracket and belt have been removed, then the pulley gear as well as the gear, etc. constituting the gear unit can possibly be separated to pieces. In such a case, assemble these parts by referring to the assembly and configuration diagram in Fig. 22.

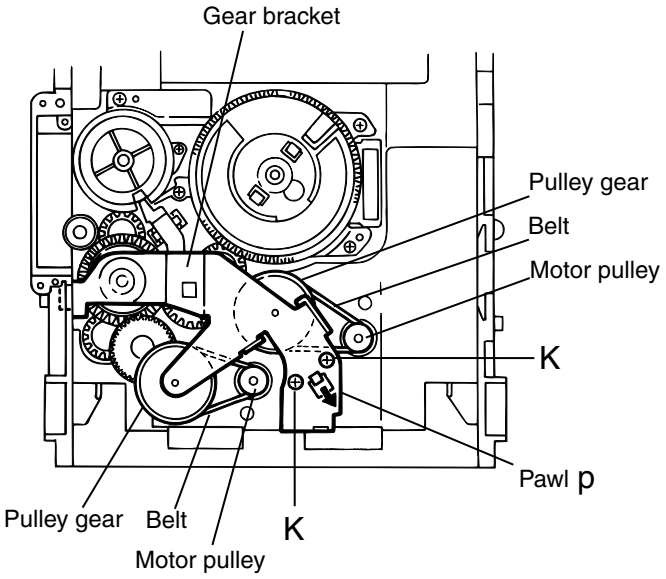


Fig.19

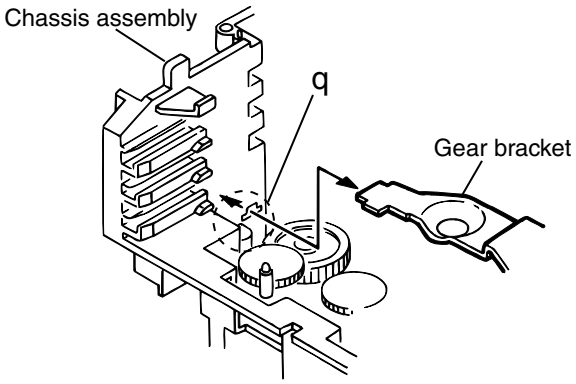


Fig.20

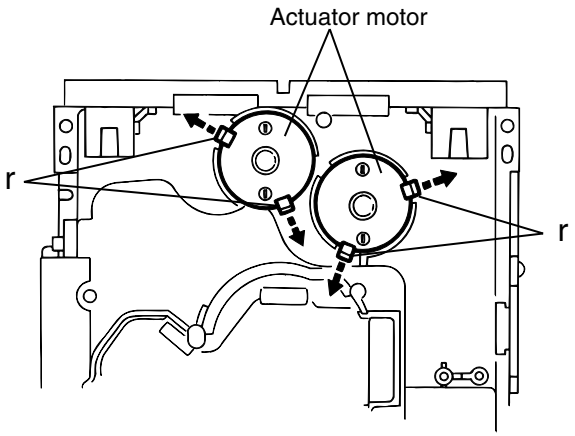


Fig.21

Assembly and Configuration Diagram

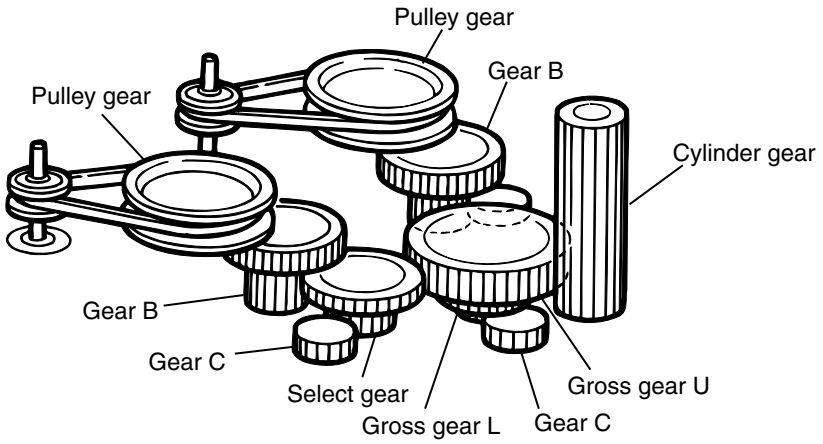


Fig.22

■ Removing the cams R1/R2 assembly and cam gear L (See Fig.23)

1. Remove the slit washer fixing the cams R1 and R2 assembly.
2. By removing the two pawls **s** fixing the cam R1, separate R2 from R1.
3. Remove the slit washer fixing the cam gear **L**.
4. Pull out the cam gear **L** from the C.G. base assembly.

■ Removing the C.G. base assembly (See Fig.23 and 24)

Remove the three screws **L** retaining the C.G. base assembly.

[Caution] To reassemble the cylinder gear, etc.with the cam unit (cam gear and cams R1/R2 assembly), gear unit and drive unit, align the position of the pawl **n** on the drive unit to that of the notch on the cam gear **L**. Then, make sure that the gear unit is engaged by turning the cam gear **L** (See Fig. 24).

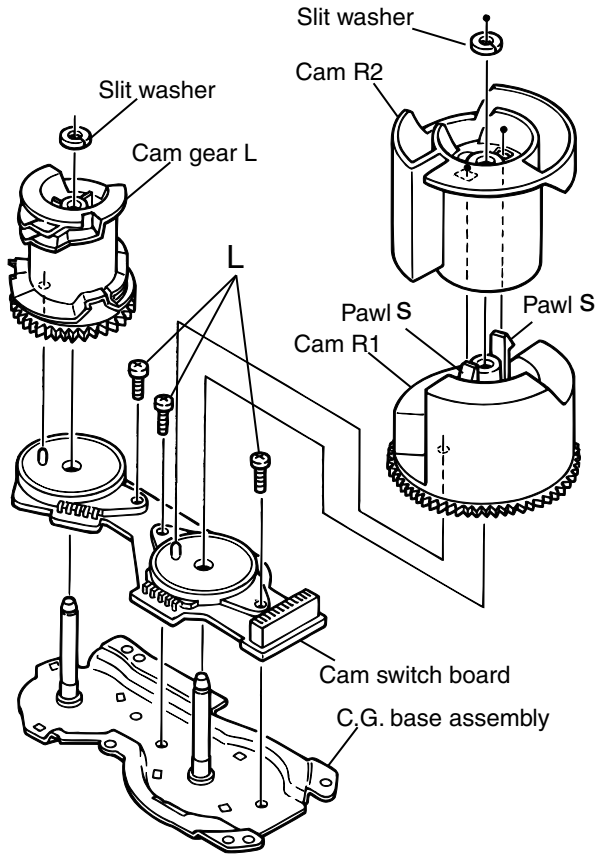


Fig.23

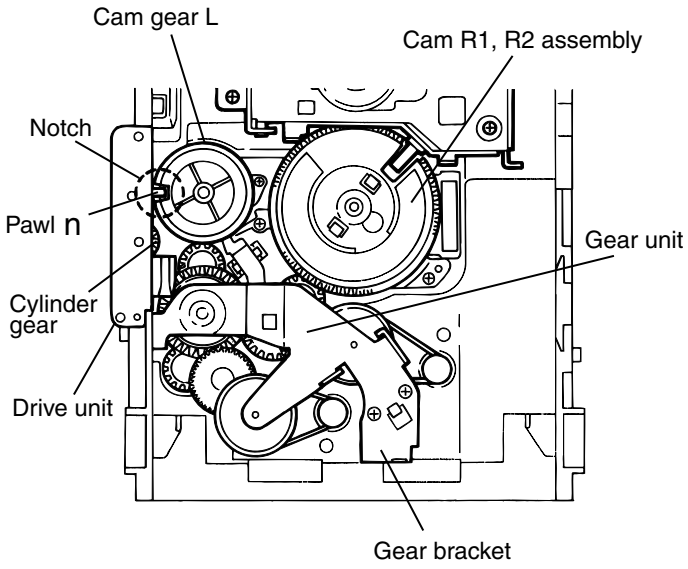


Fig.24

< DVD Traverse mechanism section>

■ Removing the pickup (See Fig.1 to 5)

1. Solder soldering **a** on the flexible board next to the pickup unit.

2. From the bottom of the traverse mechanism unit, disconnect the flexible wire from CN12 on the pickup board.

ATTENTION

The laser diode of the pick-up might be destroyed by static electricity, and solder with part a, please before extracting a flexible wire from connector (CN12). Moreover, please remove solder in part a after inserting a flexible wire in connector (CN12).
Please refer to page 1-4 for a detailed content.

3. Remove the screw **A** attaching the shaft stopper (R) on the upper side of the traverse mechanism unit. Pull the side of the shaft stopper (R) outward to release the joint **b** and remove it upward. Remove the skew spring at the same time.

4. Move the shaft in the direction of the arrow to release it from the part **c**.

5. Release the joint **d** with the shaft and remove the pickup with the shaft.

6. Pull out the shaft.

7. Remove the screw **B** attaching the switch actuator.

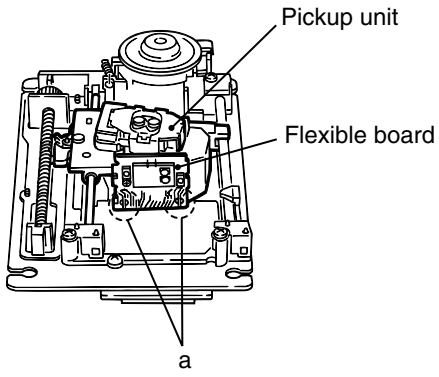


Fig.1

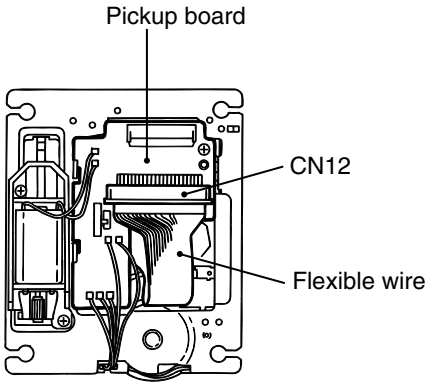


Fig.2

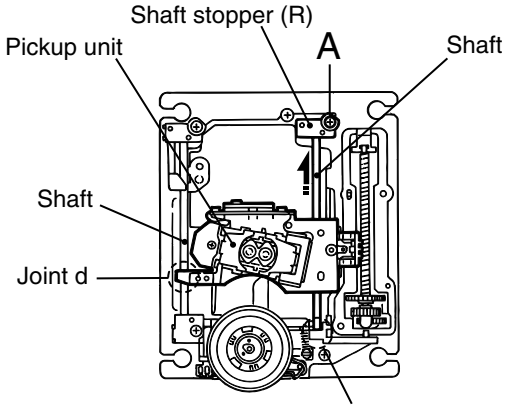


Fig.3

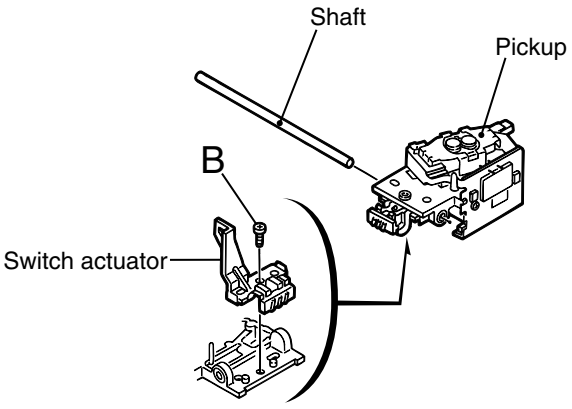


Fig.5

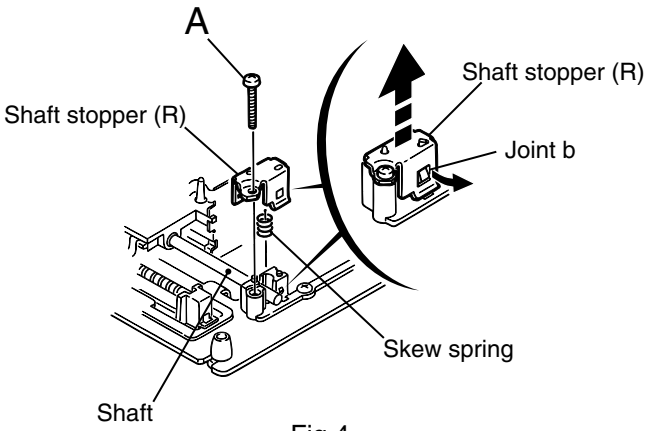


Fig.4

■Removing the pickup board
(See Fig.1 and 6)

1. Solder soldering **a** on the flexible board next to the pickup unit.

2. From the bottom of the traverse mechanism unit, disconnect the flexible wire from CN12 on the pickup board.

ATTENTION
The laser diode of the pick-up might be destroyed by static electricity, and solder with part a, please before extracting a flexible wire from connector (CN12). Moreover, please remove solder in part a after inserting a flexible wire in connector (CN12).
Please refer to page 1-4 for a detailed content.

3. Unsolder soldering **e**, **f** and **g** of each harness on the pickup board.

4. Remove the screw **C** attaching the pickup board and release the two joints **h**.

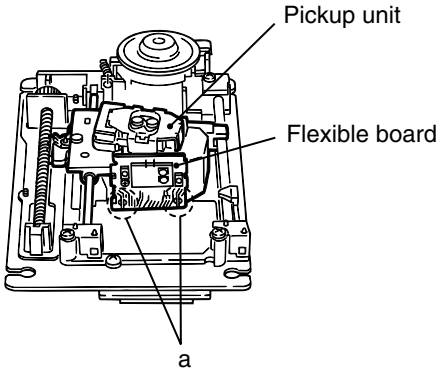


Fig.1

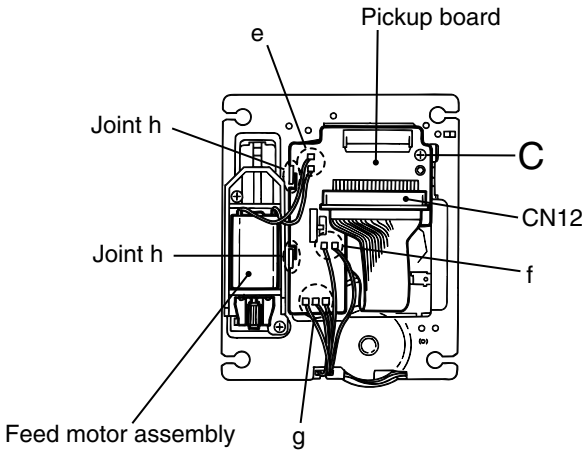


Fig.6

■Removing the feed motor assembly
(See Fig.1, 6 and 7)

1. Solder soldering **a** on the flexible board next to the pickup unit.

2. From the bottom of the traverse mechanism unit, disconnect the flexible wire from CN12 on the pickup board.

ATTENTION
The laser diode of the pick-up might be destroyed by static electricity, and solder with part a, please before extracting a flexible wire from connector (CN12). Moreover, please remove solder in part a after inserting a flexible wire in connector (CN12).
Please refer to page 1-4 for a detailed content.

3. Unsolder soldering **e** of the motor harness on the pickup board.

4. Remove the two screws **D** attaching the feed motor assembly and remove the thrust spring. Move the feed motor assembly in the direction of the arrow to pull it out from the feed holder.

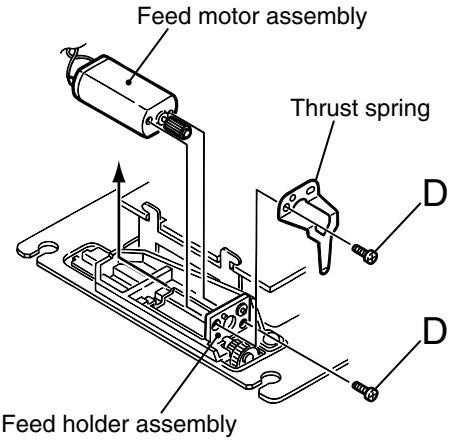


Fig.7

■ Removing the turn table assembly (See Fig.1, 6, 8 and 9)

1. Solder soldering **a** on the flexible board next to the pickup unit.

2. From the bottom of the traverse mechanism unit, disconnect the flexible wire from CN12 on the pickup board.

ATTENTION

The laser diode of the pick-up might be destroyed by static electricity, and solder with part a, please before extracting a flexible wire from connector (CN12). Moreover, please remove solder in part a after inserting a flexible wire in connector (CN12).
Please refer to page 1-4 for a detailed content.

3. Unsolder soldering **f** and **g** of the harness extending from the turn table assembly to the pickup board.

4. Remove the screw **E** attaching the shaft stopper (F) on the upper side of the traverse mechanism unit. Pull the side of the shaft stopper (F) outward to release the joint **i** and remove it upward. Remove the spring at the same time.

5. Remove the screw **F** attaching the turn table assembly.

6. Move the turn table assembly outward and pull out from the shaft. Then remove it from the base chassis.

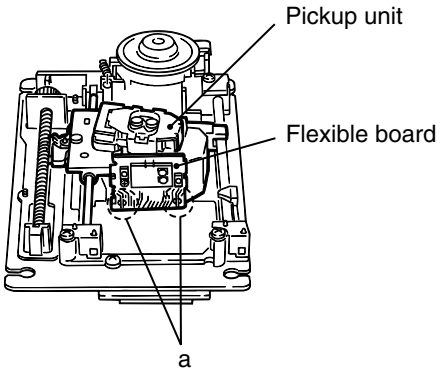


Fig.1

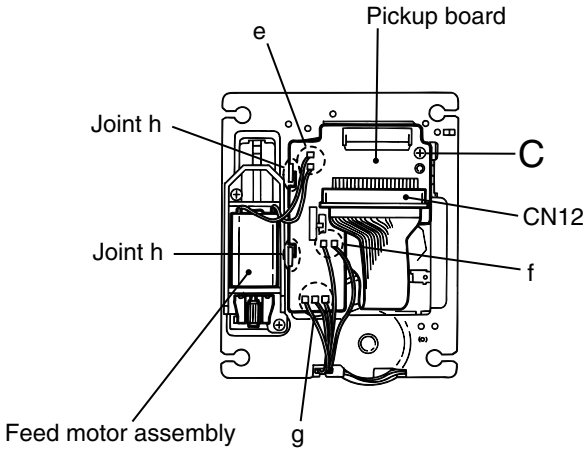


Fig.6

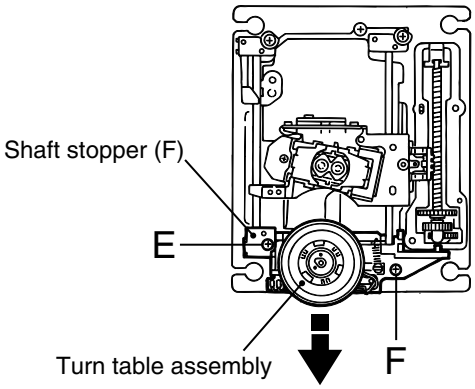


Fig.8

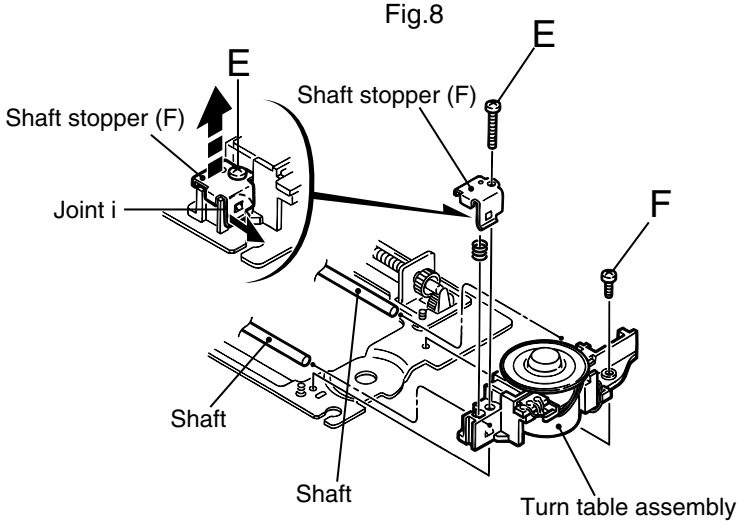


Fig.9

Adjustment method

(1) Initialization method

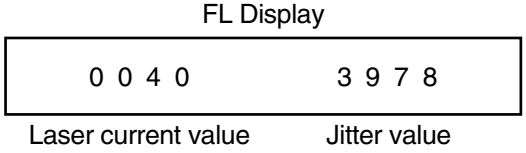
If microprocessor (IC401,IC402,IC403) or pick-up is replaces, initialize the DVD player in the following matter

1)Take out the disc and close the tray.
2)Unplug the power plug.
3)Insert power plug into outlet while pressing both PLAY button and DISC 1 OPEN/CLOSE button.
4)FL Display indicate "tESt ＊＊ ¥. ＊＊:Version, ¥Region code
5)Press 3D-PHONIC key button of remote controller. and EEPROM initialize start.
6)When indicate "V.REPLACE" on the display, initialize finishes.
7)The power is turned OFF, and Unplug the power plug.

(2) Display of "Laser current value" and "Jitter value"

"Laser current value" and "Jitter value" are displayed on the FL display by the undermentioned method. Please refer to the failure diagnosis.

1)Take out the disc and close the tray.
2)Unplug the power plug.
3)Insert power plug into outlet while pressing both PLAY button and DISC 1 OPEN/CLOSE button.
4)FL Display indicate "tESt ＊＊ ¥. ＊＊:Version, ¥Region code
5)Press the "OPEN/CLOSE" button to move the tray outward.
Put the test disc (VT-501) on the tray and press "OPEN/CLOSE" button.
The tray should move inward (Note:Don't push to close the tray directly by hand etc.)
6)Press the "PLAY" button.
7)The laser current value and the jitter value is displayed on the FL indicator as follows.



* The test mode is canceled when the power is turned off.

■ For Laser current value

The laser current value becomes 40mA for the above-mentioned.
Becomes a test mode by doing above-mentioned procedure 1) - 4). Afterwards, the laser current value can be switched by pushing the key to remote control without turning on the disk.

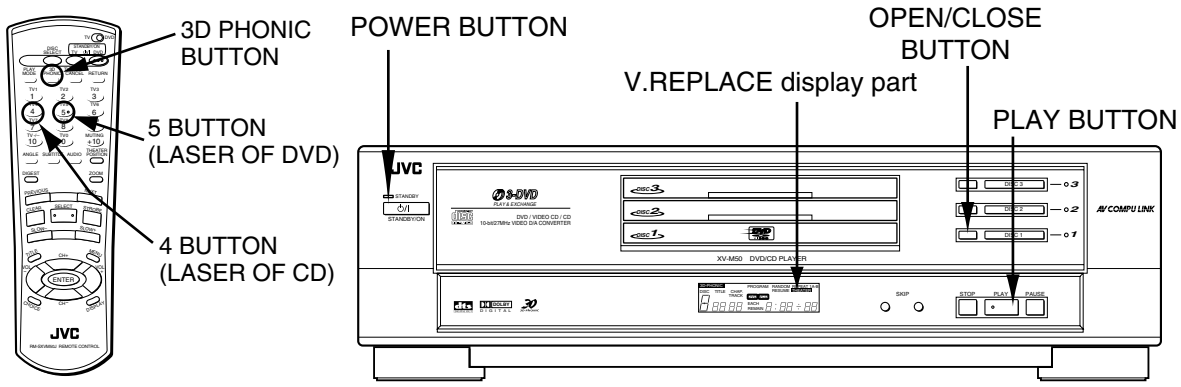
Remote control "4" key --- Laser of CD
Remote control "5" key --- Laser of DVD

*Returns to a usual test mode by the thing to push the stop button of remote control.

If the laser current value is 64mA or less, it is roughly good. There is a possibility to which pick-up is deteriorated, and exchange pick-up, please when there are 65mA or more laser current value.

■ For Jitter value

The jitter value is displayed by the hexadecimal number and refer to the conversion table of following,please.
If the indication value is 11% or less, it can be judged by this simple checking method that the signal read precision of the set is satisfactory.
Before using the TEST disc VT-501, careful check it if there is neither damage nor dirt on the read surface.



■ Jitter value

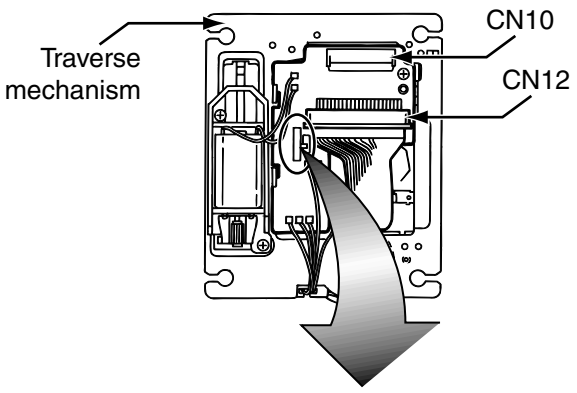
FL display	Conversion value(&)	FL display	Conversion value(&)
3818	4.7	3998	7.6
3828	4.8	39A8	7.7
3838	4.9	39B8	7.8
3848	5.1	39C8	7.9
3858	5.2	39D8	8.1
3868	5.3	39E8	8.2
3878	5.4	39F8	8.3
3888	5.5	3A18	8.5
3898	5.7	3A28	8.7
38A8	5.8	3A38	8.8
38b8	5.9	3A48	8.9
38c8	6.0	3A58	9.0
38d8	6.1	3A68	9.1
38E8	6.3	3A78	9.3
38F8	6.4	3A88	9.4
3918	6.6	3A98	9.5
3928	6.7	3AA8	9.6
3938	6.9	3AB8	9.7
3948	7.0	3AC8	9.9
3958	7.1	3AD8	10.0
3968	7.2	3AE8	10.1
3978	7.3	3AF8	10.2
3988	7.5		

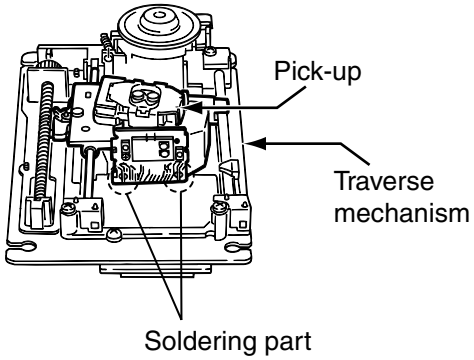
FL display	Conversion value(&)	FL display	Conversion value(&)
3B18	10.5	3C98	13.3
3B28	10.6	3CA8	13.5
3B38	10.7	3CB8	13.6
3B48	10.8	3CC8	13.7
3B58	10.9	3CD8	13.8
3B68	11.1	3CE8	13.9
3B78	11.2	3CF8	14.1
3B88	11.3	3D18	14.3
3B98	11.4	3D28	14.4
3BA8	11.5	3D38	14.5
3BB8	11.7	3D48	14.7
3BC8	11.8	3D58	14.8
3BD8	11.9	3D68	14.9
3BE8	12.0	3D78	15.0
3BF8	12.1	3D88	15.1
3C18	12.4	3D98	15.3
3C28	12.5	3DA8	15.4
3C38	12.7	3DB8	15.5
3C48	12.7	3DC8	15.6
3C58	12.9	3DD8	15.7
3C68	13.0	3DE8	15.9
3C78	13.1	3DF8	16.0
3C88	13.2		

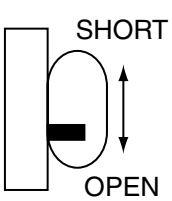
When replacing a pickup etc., execute the following adjustments:

Pickup replacement

1. When removing the traverse mechanism from the changer mechanism unit, move the pickup to the innermost diameter of the disc and set switch (S11) on the pick-up board on "SHORT" side, please before removing the card wire from connector (CN10)
2. Take out the traverse mechanism.
3. First short-circuit the pickup circuit before removing the pickup. Then carry out the replacement.







Adjustment

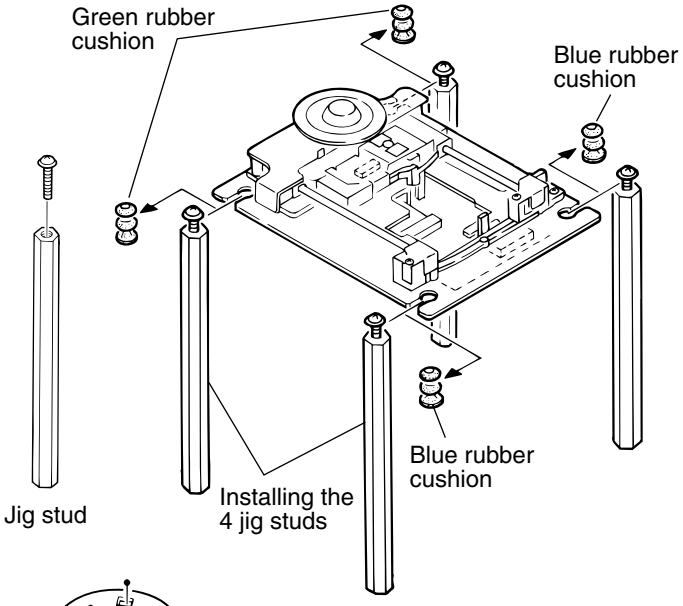
Jig setup

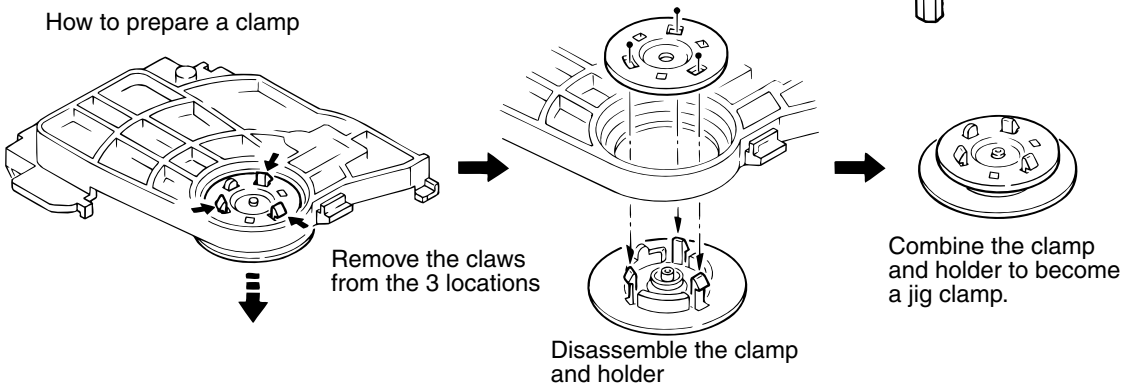
1. Remove the rubber cushion from each of the four corners of the traverse mechanism.
   (When installing be sure not to make a mistake with the cushion colors).
2. Install the jig stud.
3. Make a jig clamp. (Remove the clamp from the set and assemble it as shown in the diagram below.

Note:

How to handle the pickup

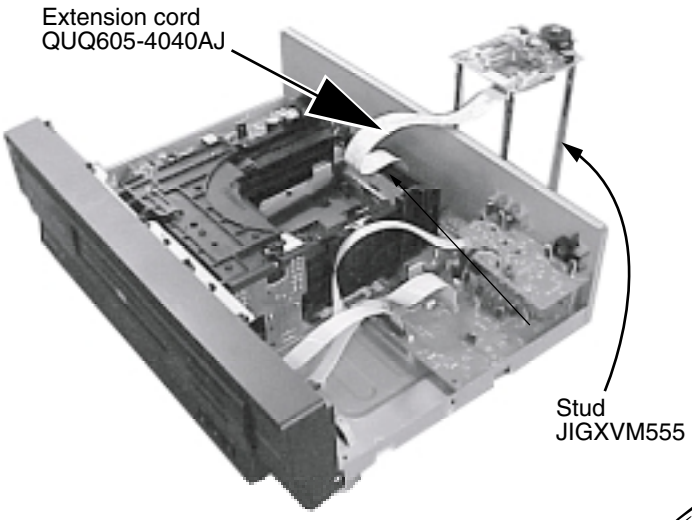
To protect the pickup from electro-static damage, make sure to hold it by the die-cast chassis (optical base). And make sure that pickup lens do not touch the top cover.





Integrated wiring for adjustment

1. Place a board on top of the unit and put the changer on it. Then carry out the wiring of the main unit.
2. Connect a extension cable to the traverse mechanism for adjustment and then connect them to the changer.
3. Remove the solder of the short-circuited flexible wire. Then remove the short-circuited pin from the traverse mechanism
4. Connection is completed.



Adjustment preparation

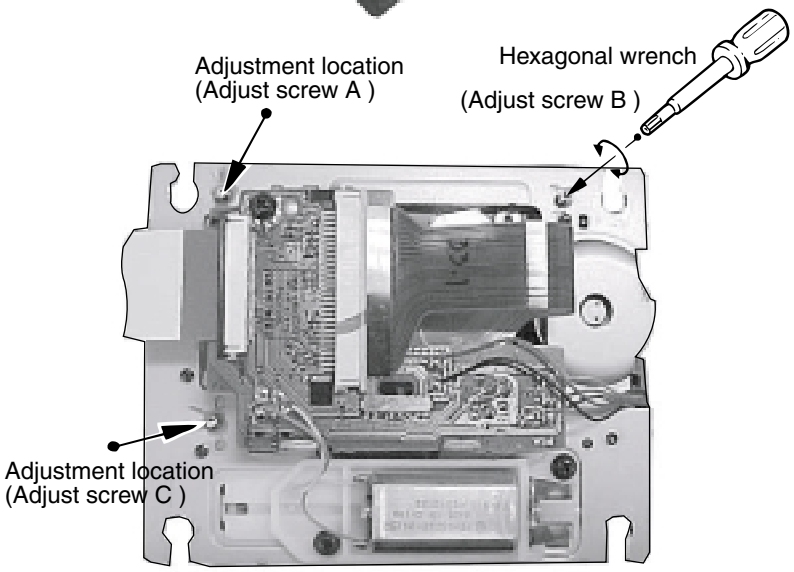
1. The 3 adjustment locations
2. 1.4 mm hexagonal wrench
3. Set the VT-501 or the VT502 test disc.

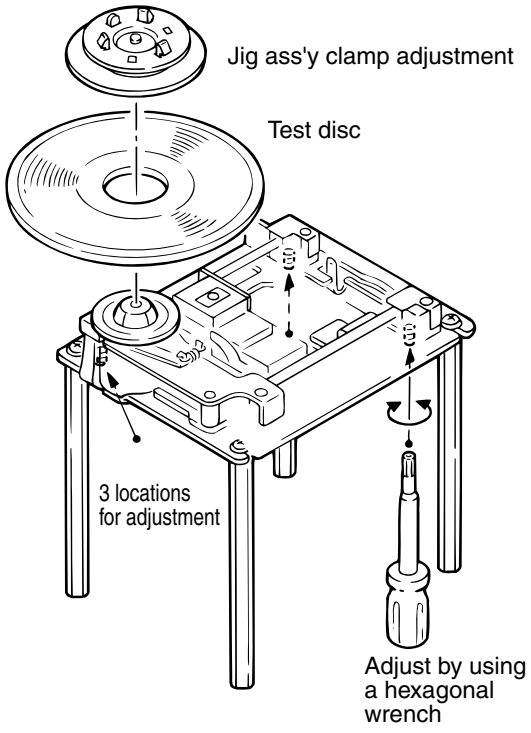
FL jitter display

1. Connect the power cable while pressing the ▲ (OPEN/CLOSE) button of DISC1 and ▷ (PLAY) button simultaneously.
   --- The DISC no. "tEStJI" is displayed on the FL indicator.
2. Press the 3D-PHONIC key button of remote controller to commence initialization.
3. When the key ▷ (PLAY) is pressed the jitter value is displayed.
4. Adjust the jitter value to minimum by using the adjust screw.

a). Turn the adjustment screw (A and B) clockwise half.
b). Return the adjustment screw (A and B) to former position.
c). Turn the adjustment screw (A and B) counterclockwise half.
d). Set the adjustment screw (A and B) to the position of best jitter at three positions.

Next, do it similar to the above-mentioned in adjustment screw A and C.

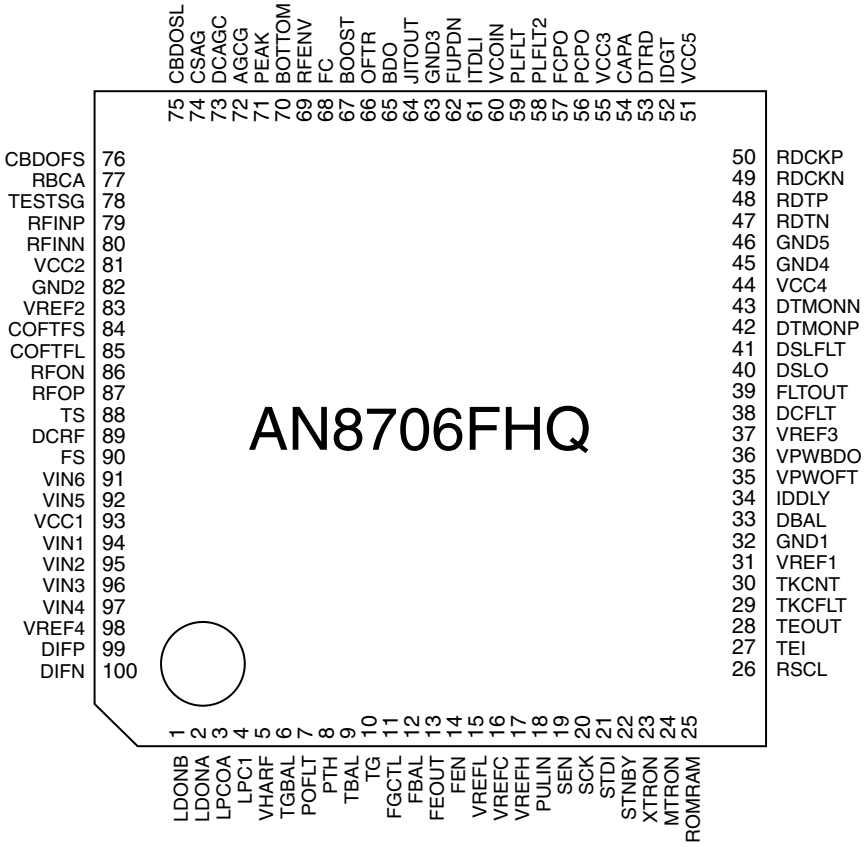




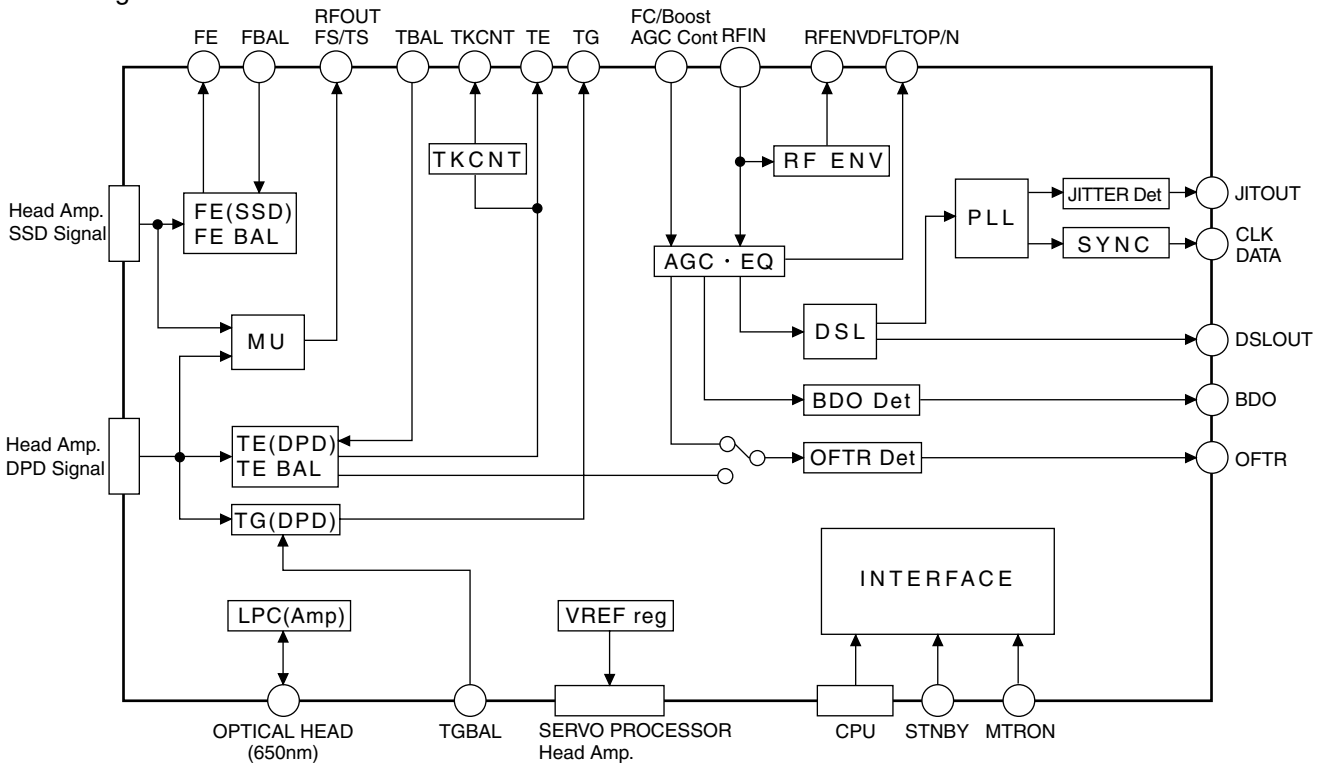
Description of major ICs

■ AN8706FHQ (IC101) : Front end processor

1.Pin layout



2.Block diagram



3.Pin function

AN8706FHQ (1/2)

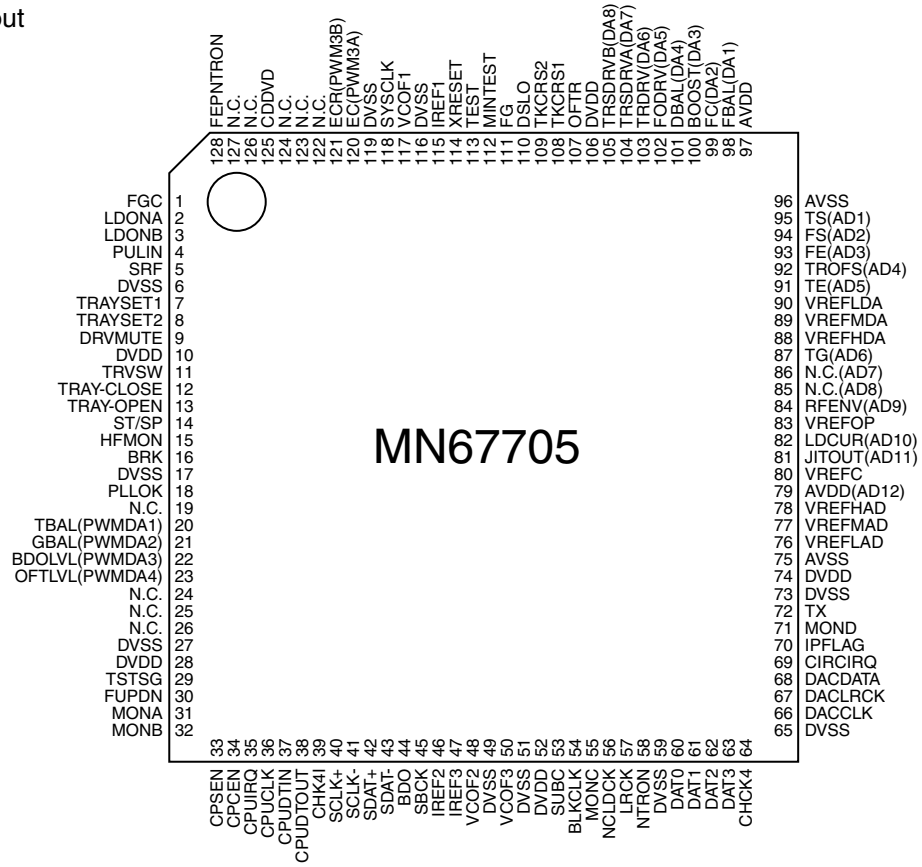
Pin No.	Symbol	I/O	Functions
1	LDONB	I	Laser ON (CD Head) terminal
2	LDONA	I	Laser ON (DVD Head) terminal
3	LPCOA	O	Laser drive output terminal
4	LPC1	I	Laser PIN input terminal
5	VHARF	O	VHALF voltage output terminal
6	TGBAL	I	Tangential phase balance control terminal
7	POFLT	O	Track detection Threshold value level terminal
8	PTH	I	Track detection Threshold value level terminal
9	TBAL	I	Tracking balance control terminal
10	TG	O	Tangential phase error signal output terminal
11	FGCTL	I	Focus amplifier Gain control terminal
12	FBAL	I	Focus balance control terminal
13	FEOUT	O	Focus error signal output terminal
14	FEN	I	Focus error output amplifier reversing input terminal
15	VREFL	O	VREFL voltage output terminal
16	VREFC	O	VREFC voltage output terminal
17	VREFH	O	VREFH voltage output terminal
18	PULIN	I	DSL,PLL drawing mode switch terminal
19	SEN	I	SEN(Cereal data input terminal)
20	SCK	I	SCK(Cereal data input terminal)
21	STDI	I	STDI(Cereal data input terminal)
22	STNBY	I	Standby mode control terminal
23	XTRON	I	Tracking OFF holding input terminal
24	MTRON	I	Monitor output ON/OFF switch terminal
25	ROMRAM	I	ROM･RAM switch terminal
26	RSCL	O	Standard current source terminal
27	TEI	I	Tracking error output amplifier reversing input terminal
28	TEOUT	O	Tracking error signal output terminal
29	TKCFLT	O	Track count detection filter terminal
30	TKCNT	O	Track count output terminal
31	VREF1	O	VREF1 voltage output terminal
32	GND1	O	Earth terminal 1
33	DBAL	I	Data slice offset adjustment terminal
34	IDDLY	I	Data slice delay adjustment terminal
35	VPWOFT	I	OFTR detection level setting terminal
36	VPWBDO	I	BDO detection level setting terminal
37	VREF3	O	VREF3 voltage output terminal
38	DCFLT	O	Capacity connection terminal for data slice input filter
39	FLTOUT	O	Filter amplifier output terminal
40	DSLO	O	Data slice single data output terminal
41	DSLFLT	O	Data slice time constant filter terminal
42	DTMONP	O	PLL differential motion 2 making to value edge signal moniter output (+)
43	DTMONN	O	PLL differential motion 2 making to value edge signal moniter output (-)
44	VCC4	I	Power terminal 4 (5V)
45	GND4	O	Earth terminal 4
46	GND5	O	Earth terminal 5
47	RDTN	O	PLL differential motion making to synchronization RF signal reversing output
48	RDTP	O	PLL differential motion making to synchronization RF signal rotation output
49	RDCKN	O	PLL differential motion making synchronization clock reversing output
50	RDCKP	O	PLL differential motion making synchronization clock rotation output

AN8706FHQ(2/2)

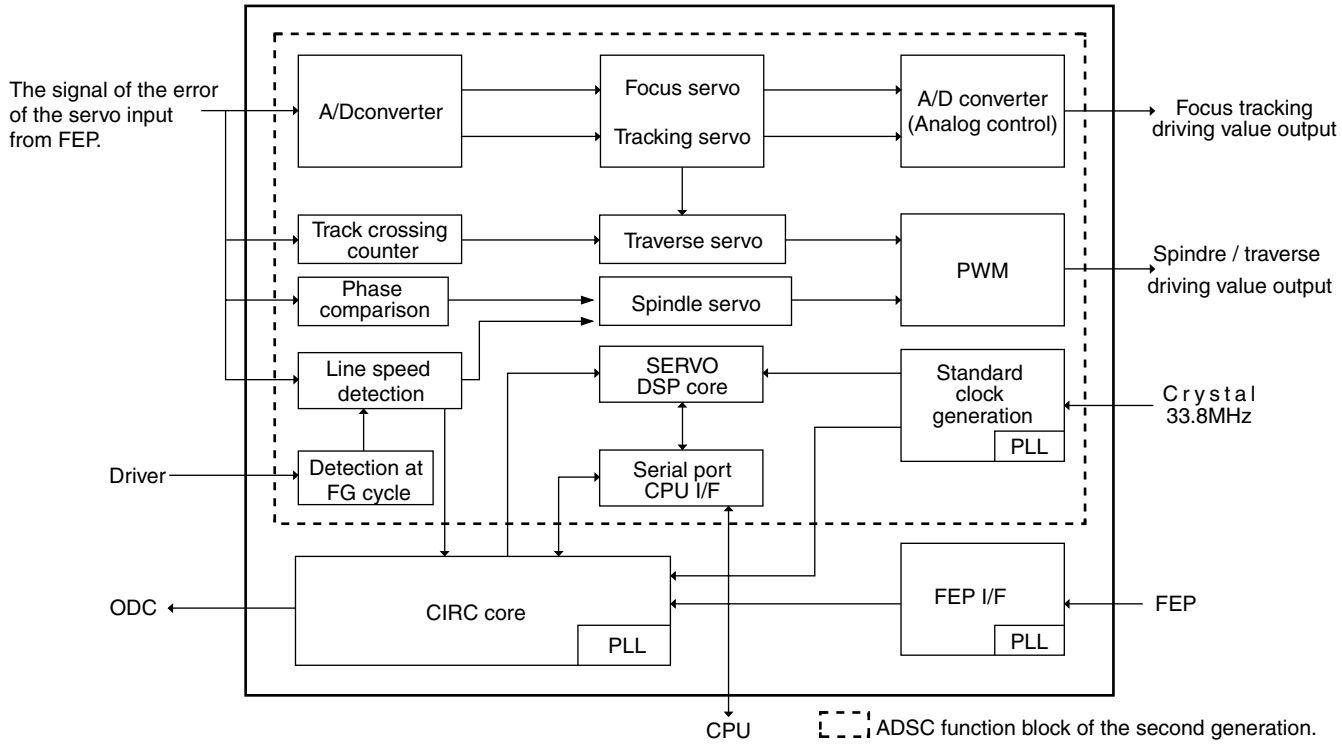
Pin No.	Symbol	I/O	Functions
51	VCC5	I	Power terminal 5 (3.3V)
52	IDGT	I	Data slice address part gate signal input terminal (For RAM)
53	DTRD	I	Data slice data read signal input terminal(For RAM)
54	CAPA	I	Data slice CAPA(Address)signal input terminal (For RAM)
55	VCC3	I	Power terminal 3 (5V)
56	PCPO	O	PLL phase gain set terminal
57	FCPO	O	PLL frequency gain set terminal
58	PLFLT2	O	PLL low-pass filter terminal
59	PLFLT	O	PLL high-pass filter terminal
60	VCOIN	I	PLL VCO input terminal
61	ITDLI	O	PLL jitter free current ripple removal filter terminal
62	FUPDN	I	PLL frequency control input terminal
63	GND3	O	Earth terminal 3
64	JITOUT	O	Detection signal output of jitter
65	BDO	O	BDO output terminal
66	OFTR	O	OFTR output terminal
67	BOOST	I	Boost control terminal for filter
68	FC	I	FC control terminal for filter
69	RFENV	O	RF envelope output terminal
70	BOTTOM	O	Bottom envelope detection filter terminal
71	PEAK	O	Peak envelope detection filter terminal
72	AGCG	O	AGC amplifier gain control terminal
73	DCAGC	O	AGC amplifier filter terminal
74	CSAG	O	Sag cancellation circuit filter terminal
75	CBDOSL	O	BDO detection capacitor terminal
76	CBDOFS	O	BDO detection capacitor terminal
77	RBCA	O	BCA detection level setting terminal
78	TESTSG	I	TEST signal input terminal
79	RFINP	I	RF signal positive input terminal
80	RFINN	I	RF signal negative input terminal
81	VCC2	I	Power terminal 2 (5V)
82	GND2	O	Earth terminal 2
83	VREF2	O	VREF2 voltage output terminal
84	COFTFS	O	OFTR detection capacitor terminal
85	COFTFL	O	OFTR detection capacitor terminal
86	RFON	O	RF signal output terminal N
87	RFOP	O	RF signal output terminal P
88	TS	O	Full adder amplifier (DVD) output terminal
89	DCRF	O	Full adder amplifier capacitor terminal
90	FS	O	Full adder amplifier (CD) output terminal
91	VIN6	I	Focus input of external division into two terminal
92	VIN5	I	Focus input of external division into two terminal
93	VCC1	I	Power terminal 1 (5V)
94	VIN1	I	External division into four (DVD/CD) RF input terminal 1
95	VIN2	I	External division into four (DVD/CD) RF input terminal 2
96	VIN3	I	External division into four (DVD/CD) RF input terminal 3
97	VIN4	I	External division into four (DVD/CD) RF input terminal 4
98	VREF4	O	VREF4 voltage output terminal
99	DIFP	O	RF signal (RAM) output terminal P
100	DIFN	O	RF signal (RAM) output terminal N

■ MN67705EA (IC201) : Digital servo controller

1.Terminal layout



2.Block diagram



3.Pin function

MN67705EA (1/3)

Pin No.	Symbol	I/O	Function
1	FGC	0	H fixation
2	LDONA	O	Laser drive controlA (ON / OFF)
3	LDONB	O	Laser drive controlB (ON / OFF)
4	PULIN	O	DSL and PLL high boost signal (FEP)
5	SRF	O	Head amplifier gain H/L selection
6	DVSS	—	Ground for digital circuit
7	TRAYSET1	O	Tray drive ON/OFF and direction control
8	TRAYSET2	O	Tray drive ON/OFF and direction control
9	DRVMUTE	O	Drive IC mute control
10	DVDD	—	Power supply for digital circuit
11	TRVSW	I	Surroundings position detection in traverse
12	TRAY-CLOSE	I	Tray close detection SW
13	TRAY-OPEN	I	Tray opening detection SW
14	ST/SP	O	Spindle motor drive switch (START /STOP)
15	HFMON	O	High cycle module control
16	BRK	O	Spindle motor IC short brake control
17	DVSS	—	Ground for digital circuit
18	PLLOK	I	SYNC detection (DVD : 18T / CD : 22T)
19	N.C.	O	
20	TBAL(PWMDA1)	O	Tracking balance (FEP)
21	GBAL(PWMDA2)	O	Tangential balance (FEP)
22	BDOLVL(PWMDA3)	O	BDO slice level (FEP)
23	OFTLVL(PWMDA4)	O	Off-track error slice level (FEP)
24	N.C.	O	
25	N.C.	O	
26	N.C.	O	
27	DVSS	—	Ground for digital circuit
28	DVDD	—	Power supply for digital circuit
29	TSTSG	O	Self calibration signal (FEP)
30	FUPDN	O	Signal of frequency UP/DOWN of PLL (FEP)
31	MONA	O	Monitor terminal A
32	MONB	O	Monitor terminal B
33	CPSEN	I	Servo DSP serial I/F chip selection (SYSCOM)
34	CPCEN	I	CIRC serial I/F chip selection (SYSCOM)
35	CPUIRQ	O	Interrupt request to silicon (SYSCOM)
36	CPUCLK	I	Silicon serial I/F clock (SYSCOM)
37	CPUDTIN	I	Silicon serial I/F data input (SYSCOM)
38	CPUDTOUT	O	Silicon serial I/F data output (SYSCOM)
39	CHK4I	I	Connects with unused DVSS
40	SCLK+	I	Lead channel clock differential motion signal (positive)
41	SCLK-	I	Lead channel clock differential motion signal (negative)
42	SDAT+	I	Lead channel data differential motion signal (positive)
43	SDAT-	I	Lead channel data differential motion signal (negative)
44	BDO	I	BDO + BCA (FEP)
45	SBCK	I	CD sub-code data shift clock (ODC)
46	IREF2	—	Connects with unused DVSS

MN67705EA (2/3)

Pin No.	Symbol	I/O	Function
47	IREF3	—	Connects with unused DVSS
48	VCOF2	—	Connects with unused DVSS
49	DVSS	—	Ground for digital circuit
50	VCOE3	—	Connects with unused DVSS
51	DVSS	—	Ground for digital cirucuit
52	DVDD	—	Power supply for digital cirucuit
53	SUBC	O	CD sub-code (ODC)
54	BLKCLK	O	CD sub-code synchronous signal (ODC)/Jump output of one at DVD
55	MONC	O	Monitor terminal C
56	NCLDCK	O	Sub-code data frame clock (ODC)
57	LRCK	O	LR channnel data strove CIRC(ODC)
58	NTRON	O	L: Tracking ON (ODC)
59	DVSS	—	Ground for digital cirucuit
60	DAT0	O	CIRC / Binary making DVD data output
61	DAT1	O	CIRC / Binary making DVD data output
62	DAT2	O	CIRC / Binary making DVD data output
63	DAT3	O	CIRC / Binary making DVD data output
64	CHCK4	O	Synchronous clock of DAT0～3
65	DVSS	—	Ground for digital circuit
66	DACCLK	O	
67	DACLRCK	I	Connects with unused DVSS
68	DACDATA	I	Connects with unused DVSS
69	CIRCIRQ	O	RAM with built-in CIRC exceeds / Underflow interrupt
70	IPFLAG	O	CIRC error flag
71	MOND	O	Monitor terminal D
72	TX	O	Digital audio interface
73	DVSS	—	Ground for digital cirucuit
74	DVDD	—	Power supply for digital cirucuit
75	AVSS	—	Ground for analog cirucuit
76	VREFLAD	—	AD subordinate position standard voltage (0.6±0.1v)
77	VREFMAD	—	It is a place standard voltage in AD (1.4±0.1V)
78	VREFHAD	—	High-ranking AD standard voltage (2.2±0.1V)
79	AVDD	—	Power supply for analog circuit
80	VREFC(AD12)	I	
81	JITOUT(AD11)	I	Jitter signal(FEP)
82	LDCUR(AD10)	I	Laser drive current signal
83	VREFOP	—	Operation amplifier standard voltage(VREFC)
84	RFENV(AD9)	I	RFENV(FEP)
85	N.C.(AD8)	I	Connects with VREFC
86	N.C.(AD7)	I	Connects with VREFC
87	TG(AD6)	I	Tangential Phase difference (FEP)
88	VREFHDA	—	High-ranking AD standard voltage (2.2±0.1V)
89	VREFMDA	—	It is a place standard voltage in AD (1.4±0.1V)
90	VREFLDA	—	AD subordinate position standard voltage (0.6±0.1v)
91	TE(AD5)	I	Tracking error (FEP)
92	TROFS(AD4)	I	Tracking drive IC input offset
93	FE(AD3)	I	Focus error (FEP)

MN67705EA (2/3)

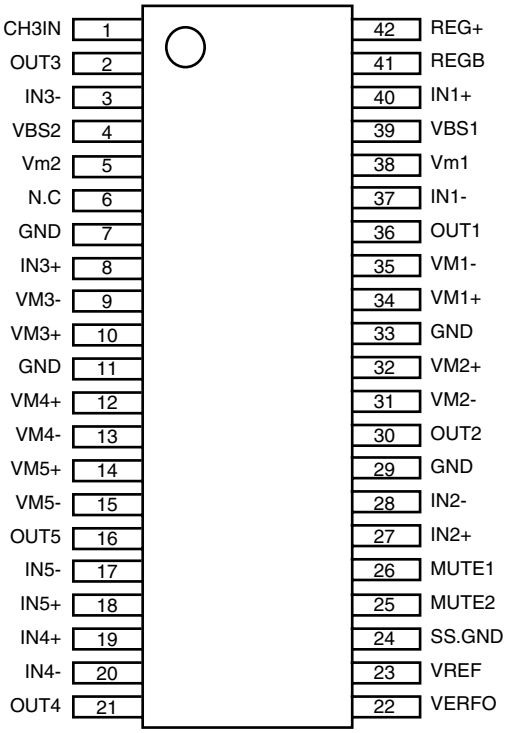
Pin No.	Symbol	I/O	Function
47	IREF3	—	Connects with unused DVSS
48	VCOF2	—	Connects with unused DVSS
49	DVSS	—	Ground for digital circuit
50	VCOE3	—	Connects with unused DVSS
51	DVSS	—	Ground for digital cirucuit
52	DVDD	—	Power supply for digital cirucuit
53	SUBC	O	CD sub-code (ODC)
54	BLKCLK	O	CD sub-code synchronous signal (ODC)/Jump output of one at DVD
55	MONC	O	Monitor terminal C
56	NCLDCK	O	Sub-code data frame clock (ODC)
57	LRCK	O	LR channnel data strove CIRC(ODC)
58	NTRON	O	L: Tracking ON (ODC)
59	DVSS	—	Ground for digital cirucuit
60	DAT0	O	CIRC / Binary making DVD data output
61	DAT1	O	CIRC / Binary making DVD data output
62	DAT2	O	CIRC / Binary making DVD data output
63	DAT3	O	CIRC / Binary making DVD data output
64	CHCK4	O	Synchronous clock of DAT0～3
65	DVSS	—	Ground for digital circuit
66	DACCLK	O	
67	DACLRCK	I	Connects with unused DVSS
68	DACDATA	I	Connects with unused DVSS
69	CIRCIRQ	O	RAM with built-in CIRC exceeds / Underflow interrupt
70	IPFLAG	O	CIRC error flag
71	MOND	O	Monitor terminal D
72	TX	O	Digital audio interface
73	DVSS	—	Ground for digital cirucuit
74	DVDD	—	Power supply for digital cirucuit
75	AVSS	—	Ground for analog cirucuit
76	VREFLAD	—	AD subordinate position standard voltage (0.6±0.1v)
77	VREFMAD	—	It is a place standard voltage in AD (1.4±0.1V)
78	VREFHAD	—	High-ranking AD standard voltage (2.2±0.1V)
79	AVDD	—	Power supply for analog circuit
80	VREFC(AD12)	I	
81	JITOUT(AD11)	I	Jitter signal(FEP)
82	LDCUR(AD10)	I	Laser drive current signal
83	VREFOP	—	Operation amplifier standard voltage(VREFC)
84	RFENV(AD9)	I	RFENV(FEP)
85	N.C.(AD8)	I	Connects with VREFC
86	N.C.(AD7)	I	Connects with VREFC
87	TG(AD6)	I	Tangential Phase difference (FEP)
88	VREFHDA	—	High-ranking AD standard voltage (2.2±0.1V)
89	VREFMDA	—	It is a place standard voltage in AD (1.4±0.1V)
90	VREFLDA	—	AD subordinate position standard voltage (0.6±0.1v)
91	TE(AD5)	I	Tracking error (FEP)
92	TROFS(AD4)	I	Tracking drive IC input offset
93	FE(AD3)	I	Focus error (FEP)

MN67705EA(3/3)

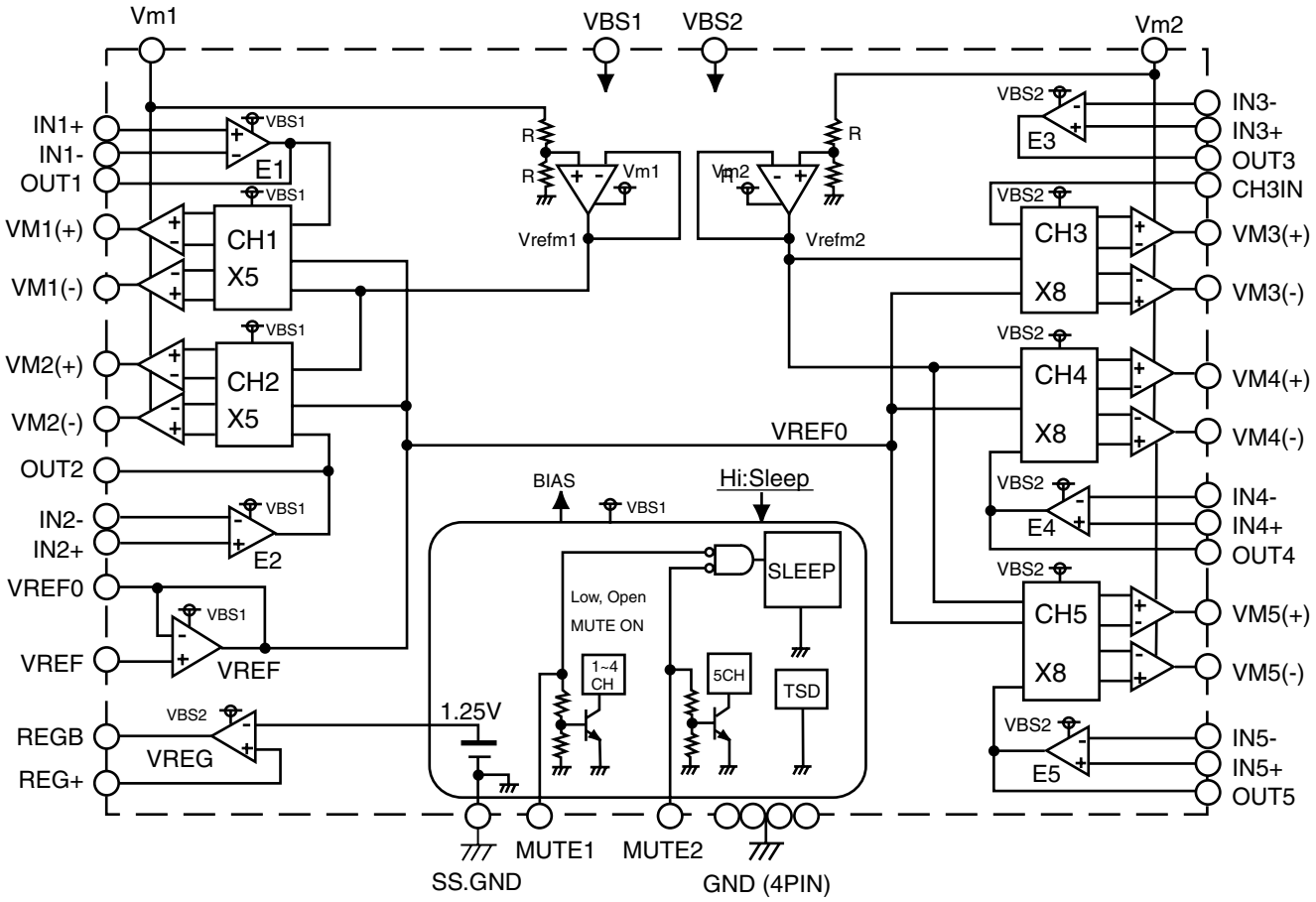
Pin No.	Symbol	I/O	Function
94	FS(AD2)	I	FS (FEP)
95	TS(AD1)	I	TS (FEP)
96	AVSS	—	Ground for analog cirucuit
97	AVDD	—	Power supply for analog circuit
98	FBAL(DA1)	O	Focus balance(FEP)
99	FC(DA2)	O	Cutting off frequency (FEP)
100	BOOST(DA3)	O	Amount of boost (FEP)
101	DBAL(DA4)	O	DSL offset balance (FEP)
102	FODRV(DA5)	O	Focus drive
103	TRDRV(DA6)	O	Tracking drive
104	TRSDRVA(DA7)	O	Traverse drive A aspect
105	TRSDRVB(DA8)	O	Traverse drive B aspect
106	DVDD	—	Power supply for digital cirucuit
107	OFTR	I	Off-track error signal (FEP)
108	TKCRS1	I	Track crossing signal 1 (FEP)
109	TKCRS2	I	Track crossing signal 2 (FEP)
110	DSLO	I	Binary making data slice signal (FEP)
111	FG	I	FG signal input (spindle motor driver)
112	MINTEST	—	Connects with DVSS
113	TEST	—	Connects with DVSS
114	XRESET	I	Reset L : Reset
115	IREF1	—	VCO reference current 1(for SYSCLK)
116	DVSS	—	Ground for digital circuit)
117	VCOF1	—	VCO control voltage 1 (for SYSCLK)
118	SYSCLK	I	33.8MHz system clock input
119	DVSS	—	Ground for digital circuit
120	EC(PWM3A)	O	Spindle motor drive
121	ECR(PWM3B)	O	
122	N.C.(PWM3A)	O	
123	N.C.(PWM2B)	O	
124	N.C.(PWM1A)	O	
125	CDDVD	O	CD/DVD control signal (FEP) CD : H DVD : L
126	N.C.(PWM0A)	O	
127	N.C.(PWM0B)	O	
128	FEPNTRON	O	Tracking ON (FEP)

M56788FP-W (IC271) : Traverse mechanism driver

1.Terminal layout

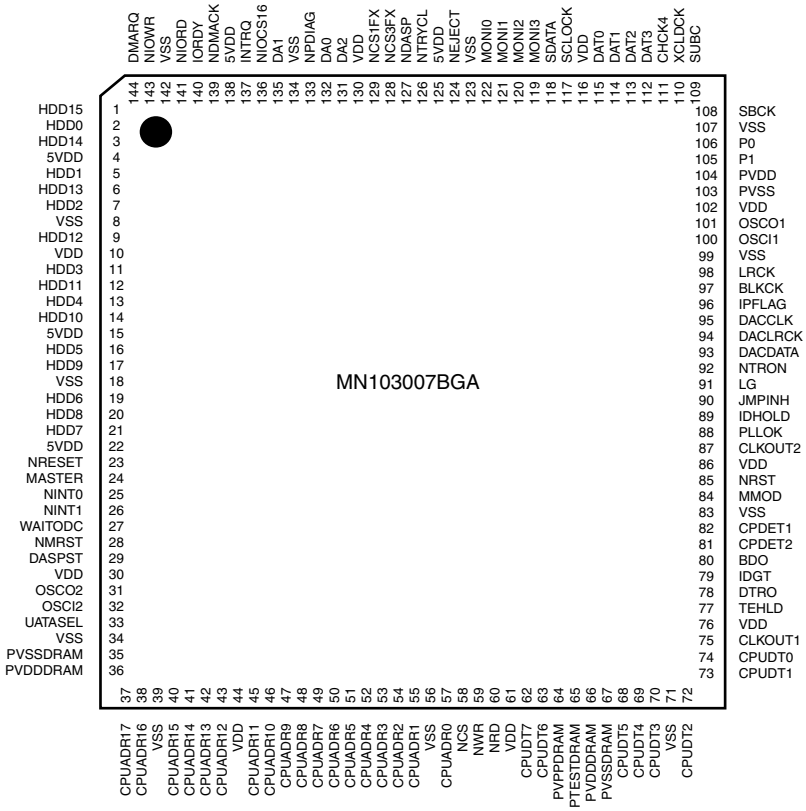


2.Block diagram

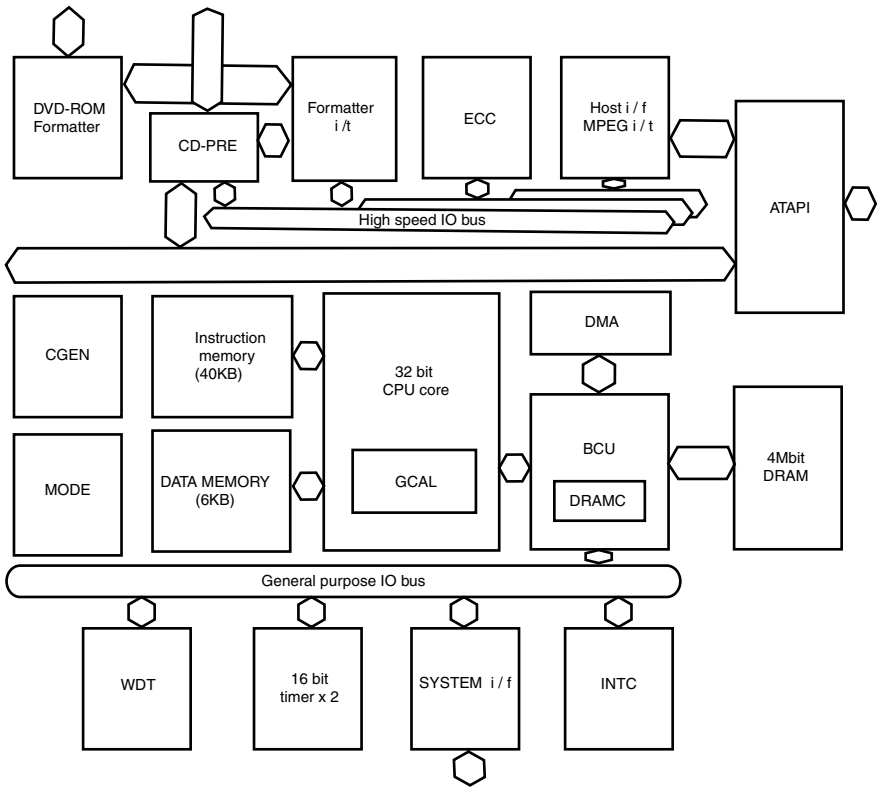


■ MN103007BGA (IC301) : Optical disc controller

1.Terminal layout



2.Block diagram



3.Pin function

MN103007BGA(1/4)

Pin NO.	Symbol	I/O	Function
1	HDD15	I/O	ATAPI data
2	HDD0	I/O	ATAPI data
3	HDD14	I/O	ATAPI data
4	5VDD		
5	HDD1	I/O	ATAPI data
6	HDD13	I/O	ATAPI data
7	HDD2	I/O	ATAPI data
8	VSS		
9	HDD12	I/O	ATAPI data
10	VDD		
11	HDD3	I/O	ATAPI data
12	HDD11	I/O	ATAPI data
13	HDD4	I/O	ATAPI data
14	HDD10	I/O	ATAPI data
15	5VDD		
16	HDD5	I/O	ATAPI data
17	HDD9	I/O	ATAPI data
18	VSS		
19	HDD6	I/O	ATAPI data
20	HDD8	I/O	ATAPI data
21	HDD7	I/O	ATAPI data
22	5VDD		
23	NRESET	I	ATAPI reset
24	MASTER	I/O	ATAPI master / slave selection
25	NINT0	O	System control interruption 0
26	NINT1	O	System control interruption 1
27	WAITODC	O	System control weight control
28	NMRST	O	System control reset
29	DASPST	I	DASP signal initializing
30	VDD		
31	OSCO2	I,O	VSS connection,OPEN
32	OSCI2	I,O	VSS connection,OPEN
33	UATASEL	I	VSS connection
34	VSS		
35	PVSSDRAM		
36	PVDDDRAM		
37	CPUADR17	I	System control address
38	CPUADR16	I	System control address
39	VSS		
40	CPUADR15	I	System control address
41	CPUADR14	I	System control address
42	CPUADR13	I	System control address
43	CPUADR12	I	System control address
44	VDD		System control address
45	CPUADR11	I	System control address

MN103007BGA(2/4)

Pin NO.	Symbol	I/O	Function
46	CPUADR10	I	System control address
47	CPUADR9	I	System control address
48	CPUADR8	I	System control address
49	CPUADR7	I	System control address
50	CPUADR6	I	System control address
51	CPUADR5	I	System control address
52	CPUADR4	I	System control address
53	CPUADR3	I	System control address
54	CPUADR2	I	System control address
55	CPUADR1	I	System control address
56	VSS		GND
57	CPUADR0	I	System control address
58	NCS	I	System control chip select
59	NWR	I	System control write
60	NRD	I	System control read
61	VDD		Apply 3V
62	CPUDT7		System control data
63	CPUDT6		System control data
64	PVPPDRAM	O	C=10000PF is connected between VSS
65	PTESTDRAM	I	VSS connected
66	PVDDDRAM		
67	PVSSDRAM		
68	CPUDT5		System control data
69	CPUDT4		System control data
70	CPUDT3		System control data
71	VSS		GND
72	CPUDT2		System control data
73	CPUDT1	I/O	System control data
74	CPUDT0	I/O	System control data
75	CLKOUT1	O	16.9/11.2/8.45MHz clock
76	VDD	-	Apply 3V
77	TEHLD	O	Mirror gate
78	DTRO	O	Data part frequency control switch
79	IDGT	O	Part CAPA switch
80	BDO	I	RF dropout / BCA data of making to binary
81	CPDET2	I	Outer side CAPA detection
82	CPDET1	I	Side of surroundings on inside
83	VSS		GND
84	MMOD	I	VSS connected
85	NRST	I	System reset
86	VDD	-	Apply 3V
87	CLKOUT2	O	16.9MHz clock
88	PLLOK	O	Frame mark detection
89	IDHOLD	O	ID gate for tracking holding
90	JMPINH	O	Jump prohibition

MN103007BGA(3/4)

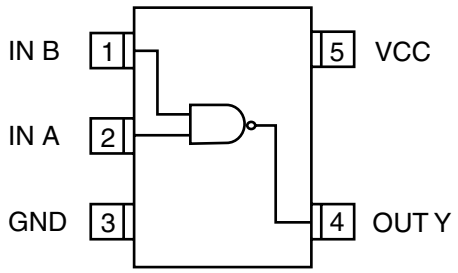
Pin NO.	Symbol	I/O	Function
91	LG	O	Land / group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Serial output
94	DACLRCK	O	L and R identification output
95	DACCLK	I	Clock for serial output
96	IPFLAG	I	Interpolation flag input
97	BLKCK	I	Sub-code,Block clock input
98	LRCK	I	L and R identification signal output
99	VSS		
100	OSCI1	I,O	16.9MHz oscillation
101	OSCO1	I,O	16.9MHz oscillation
102	VDD		
103	PVSS		
104	PVDD		
105	P1	I/O	Terminal MASTER polarity switch input
106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input
107	VSS		
108	SBCK	O	Sub-code, Clock output for serial input
109	SUBC	I	Sub-code, Serial input
110	XCLDCK	I	Sub-code, Frame clock input
111	CHCK4	I	Read clock to DAT3~0 (Output of dividing frequency four from ADSC)
112	DAT3	I	Read data from DISC (Parallel output from ADSC)
113	DAT2	I	
114	DAT1	I	
115	DAT0		
116	VDD		
117	SCLOCK	I/O	Debugging serial clock (270Ω pull up)
118	SDATA	I/O	Debugging serial data (270Ω pull up)
119	MONI3	O	Internal goods title monitor
120	MONI2	O	
121	MONI1	O	
122	MONI0	O	
123	VSS		
124	NEJECT	I	Eject detection
125	5VDD		
126	NTRYCL	I	Tray close detection
127	NDASP	I/O	ATAPI Drive active/ Slave connection I/O
128	NCS3FX	I	ATAPI host chip select
129	NCS1FX	I	ATAPI host chip select
130	VDD		
131	DA2	I/O	ATAPI host address
132	DA0	I/O	ATAPI host address

MN103007BGA(4/4)

Pin NO.	Symbol	I/O	Function
133	NPDIAG	I/O	ATAPI slave master diagnosis input
134	VSS		
135	DA1	I/O	ATAPI host address
136	NIOCS16	O	ATAPI output of selection of width of host data bus
137	INTRQ	O	ATAPI host interruption output
138	5VDD		
139	NDMACK	I	ATAPI host DMA response
140	IORDY	O	ATAPI host ready output
141	NIORD	I	ATAPI host read
142	VSS		
143	NIOWR	I/O	ATAPI host write
144	DMARQ	O	ATAPI host DMA demand

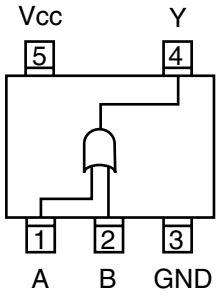
■ TC7SH08FU-X (IC311) : Timing control

1.Terminal layout



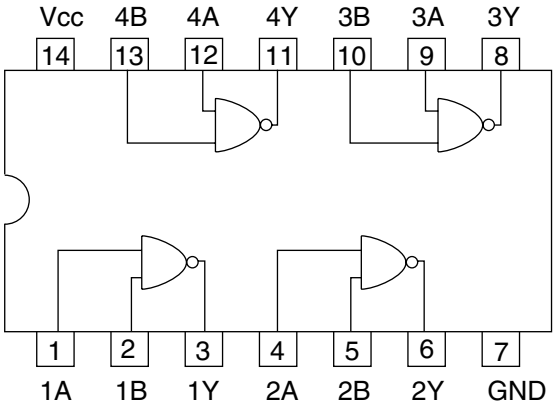
■ TC7SH32FU-X (IC312) : 2 Input Single OR Gate

1.Terminal layout



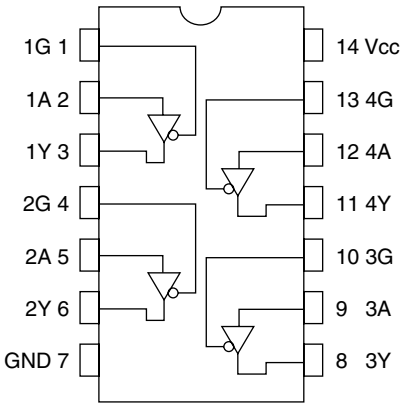
■ TC74VHC00FT-X (IC322,IC503) : Write timing control

1.Terminal layout / Block diagram



■ TC74VHC125FT-X (IC411) : Buffer

1. Pin layout & block diagram



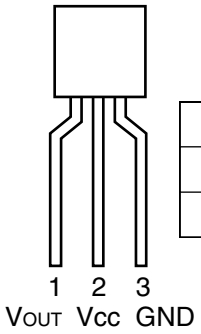
2. Truth table

INPUTS		OUTPUTS
$\overline{G}$	A	Y
H	X	Z
L	L	L
L	H	H

X: Don't care
Z:High impedance

■ IC-PST9140-T (IC702) : SYSTEM RESET

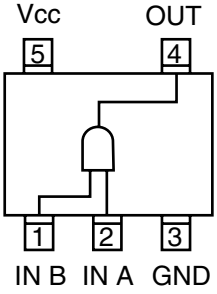
1.Terminal layout



1	VOUT
2	Vcc
3	GND

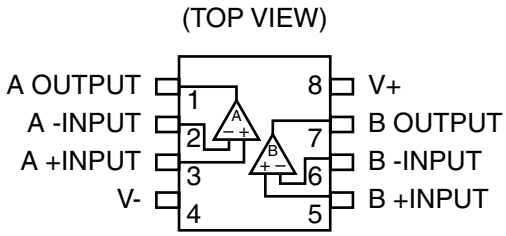
■ TC7S07F-W (IC704) : 2 Input Single AND Gate

1.Terminal layout



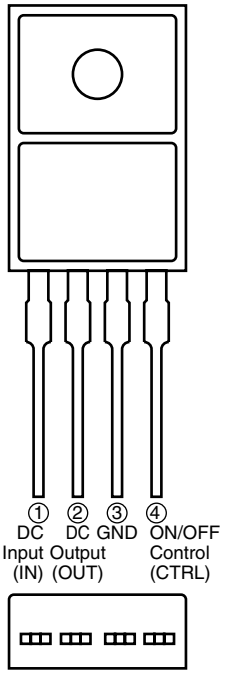
■ NJM4580M-X (IC741,IC751) : Dual Operational Amplifier

1.Terminal layout



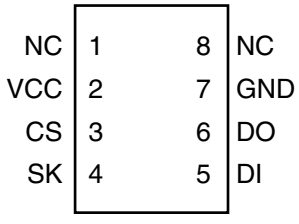
■ PQ05RD21 (IC951) : Regulator

1.Terminal layout



■ BR93LC66F-X(IC403):EEPROM

1.Terminal layout

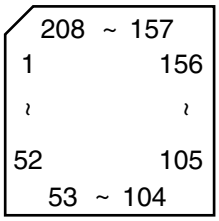


2.Pin Functions

Symbol	I/O	Function
VCC	-	Power supply
GND	-	Connect to GND
CS	I	Chip select input
SK	I	Serial clock input
DI	I	Start bit,OP-code,address,serial data input
DO	O	Serial data output, Internal state display output of READY/BUSY

■ ZIVA-4.1-PA2(IC501):Back end - Digital decoder

1.Terminal layout



2.Pin function (1/5)

Pin No.	Symbol	I/O	Description
1	RD	I	Read strobe input
2	R/W	I	Read/write strobe input
3	VDD	-	Power supply terminal 3.3V
4	WAIT	O	Transfer not complete / data acknowledge. Active LOW to indicate host initiated transfer is complete.
5	RESET	I	Active LOW : reset signal input
6	VSS	-	Connect to ground
7	VDD	-	Power supply terminal 3.3V
8	INT	O	Host interrupt signal output
9	NC	-	Non connect
10	NC	-	Non connect
11	NC	-	Non connect
12	NC	-	Non connect
13	VDD	-	Power supply terminal 2.5V
14	VSS	-	Connect to ground
15	NC	-	Non connect
16	NC	-	Non connect
17	NC	-	Non connect
18	NC	-	Non connect
19	VSS	-	Connect to ground
20	VDD	-	Power supply 3.3V
21	VDATA0	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
22	VDATA1	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
23	VDATA2	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
24	VDATA3	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
25	VDATA4	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
26	VDATA5	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
27	VDATA6	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
28	VDATA7	O	Video data bus output. Byte serial CbYCrY data synchronous with VCLK.
29	VSYNC	I/O	Vertical sync. Bi-directional, the decoder output the top border of a new field on the first HSYNC after the falling edge of VSYNC.
30	HSYNC	I/O	Horizontal sync. The decoder begins outputting pixel data for a new horizontal line after the falling (active) edge of HSYNC.
31	VSS	-	Connect to ground
32	VDD	-	Power supply terminal 3.3V
33	NC	-	Non connect
34	NC	-	Non connect
35	NC	-	Non connect
36	VDD	-	Power supply terminal 2.5V

2.Pin function (2/5)

Pin No.	Symbol	I/O	Description
37	VSS	-	Connect to ground
38	NC	-	Non connect
39	NC	-	Non connect
40	NC	-	Non connect
41	NC	-	Non connect
42	NC	-	Non connect
43	PIO0	I/O	Programmable I/O terminal
44	VSS	-	Connect to ground
45	VDD	-	Power supply terminal 3.3V
46	PIO1	I/O	Programmable I/O terminal
47	PIO2	I/O	Programmable I/O terminal
48	PIO3	I/O	Programmable I/O terminal
49	PIO4	I/O	Programmable I/O terminal
50	PIO5	I/O	Programmable I/O terminal
51	PIO6	I/O	Programmable I/O terminal
52	PIO7	I/O	Programmable I/O terminal
53	MDATA0	I/O	SDRAM data
54	MDATA1	I/O	SDRAM data
55	VDD	-	Power supply terminal 3.3V
56	VSS	-	Connect to ground
57	MDATA2	I/O	SDRAM data
58	MDATA3	I/O	SDRAM data
59	MDATA4	I/O	SDRAM data
60	MDATA5	I/O	SDRAM data
61	MDATA6	I/O	SDRAM data
62	MDATA7	I/O	SDRAM data
63	MDATA15	I/O	SDRAM data
64	VDD	-	Power supply terminal 3.3V
65	VSS	-	Connect to ground
66	MDATA14	I/O	SDRAM data
67	VDD	-	Power supply terminal 2.5
68	VSS	-	Connect to ground
69	MDATA13	I/O	SDRAM data
70	MDATA12	I/O	SDRAM data
71	MDATA11	I/O	SDRAM data
72	MDATA10	I/O	SDRAM data
73	MDATA9	I/O	SDRAM data
74	VDD	-	Power supply terminal 3.3V
75	VSS	-	Connect to ground
76	MDATA8	I/O	SDRAM data
77	LDQM	O	SDRAM Lower or upper mask
78	SD-CLK	O	SDRAM Clock
79	CLKSEL	I	Selects SYSCLK or VCLK as clock source. Normal operation is to tie HIGH.
80	MADDR9	O	SDRAM address
81	MADDR8	O	SDRAM address
82	VDD	-	Power supply terminal 3.3V
83	VSS	-	Connect to ground
84	MADDR7	O	SDRAM address

2.Pin function (3/5)

Pin No.	Symbol	I/O	Description
85	MADDR6	O	SDRAM address
86	MADDR5	O	SDRAM address
87	VDD	-	Power supply terminal 2.5V
88	VSS	-	Connect to ground
89	MADDR4	O	SDRAM address
90	MWE	O	SDRAM write enable
91	SD-CAS	O	Active LOW SDRAM column address
92	VDD	-	Power supply terminal 3.3V
93	VSS	-	Connect to ground
94	SD-RAS	O	Active LOW SDRAM row address
95	SD-CS0	O	Active LOW SDRAM chip select 0
96	SD-CS1/MADDR11	O	Active LOW SDRAM chip select 1 or use as MADDR11 for larger SDRAM
97	SD-BS	O	SDRAM bank select
98	MADDR10	O	SDRAM address
99	MADDR0	O	SDRAM address
100	VDD	-	Power supply terminal 3.3V
101	VSS	-	Connect to ground
102	MADDR1	O	SDRAM address
103	MADDR2	O	SDRAM address
104	MADDR3	O	SDRAM address
105	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
106	NC	-	Non connect
107	NC	-	Non connect
108	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
109	NC	-	Non connect
110	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
111	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
112	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table1
113	DAI-LRCK	I	PCM left/right clock
114	DAI-BCK	I	PCM input bit clock
115	VDD	-	Power supply 3.3V
116	VSS	-	Connect to ground
117	DAI-DATA	I	PCM data input
118	DA-DATA3	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
119	DA-DATA2	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
120	DA-DATA1	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
121	DA-DATA0	O	PCM data output. Eight channels. Serial audio samples relative to DA_BCK and DA_LRCK
122	DA-LRCK	O	PCM left clock. Identifies the channel for each sample
123	VDD	-	Power supply terminal 3.3V
124	VSS	-	Connect to ground
125	DA-XCK	I/O	Audio external frequency clock input or output
126	DA-BCK	O	PCM bit clock output
127	DA-IEC	O	PCM data out in IEC-958 format or compressed data out in IEC-1937 format
128	VDD	-	Power supply terminal 2.5V

2.Pin function (4/5)

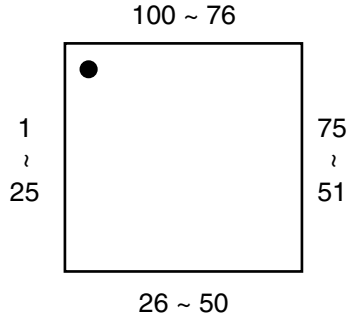
Pin No.	Symbol	I/O	Description
129	VSS	-	Connect to ground
130	NC	-	Non connect
131	VSS_DAC	-	Connect to ground for analog video DAC
132	VSS_VIDEO	-	Connect to ground for analog video
133	CVBS	O	DAC video output format : CVBS. Macrovision encoded
134	VDD_DAC	-	Power supply terminal for analog video DAC
135	VDD_VIDEO	-	Power supply terminal for analog video
136	NC	-	Non connect
137	VSS_DAC	-	Connect to ground for analog video DAC
138	VSS_VIDEO	-	Connect to ground for analog video
139	CVBS/G/Y	O	DAC video output format. Macrovision encoded
140	VDD_DAC	-	Power supply terminal for analog video DAC
141	VDD_VIDEO	-	Power supply terminal for analog video
142	NC	-	Non connect
143	VSS_DAC	-	Connect to ground for analog video DAC
144	VSS_VIDEO	-	Connect to ground for analog video
145	Y/B/U	O	DAC video output format. Macrovision encoded
146	VDD_DAC	-	Power supply terminal for analog video DAC
147	VDD_VIDEO	-	Power supply terminal for analog video
148	NC	-	Non connect
149	VSS_DAC	-	Connect to ground for analog video DAC
150	VSS_VIDEO	-	Connect to ground for analog video
151	C/R/V	O	DAC video output format. Macrovision encoded
152	VDD_DAC	-	Power supply terminal for analog video DAC
153	VDD_VIDEO	-	Power supply terminal for analog video
154	VSS_RREF	-	Connect to ground for analog video
155	RREF	O	Reference resistor. Connecting to pin 154
156	VDD_RREF	-	Power supply terminal for analog video 3.3V
157	A_VSS	-	Power supply terminal for analog PLL 3.3V
158	SYSCLK	I	Optical system clock. Tie to A_VDD through a 1K ohm resistor
159	VCLK	I	System clock input
160	A_VDD	-	Power supply terminal for analog PLL 3.3V
161	DVD-DATA0/CD-DATA	I	Serial CD data. This pin is shared with DVD compressed data DVD-DATA0
162	DVD-DATA1/CD-LRC	I	Programmable polarity 16-bit word synchronization to the decoder. This pin is shared with DVD compressed data DVD-DATA1
163	DVD-DATA2/CD-BCK	I	CD bit clock. Decoder accept multiple BCK rates. This pin is shared with DVD compressed DVD-DATA2
164	DVD-DATA3/CD-C2PO	I	Asserted HIGH indicates a corrupted byte. This pin is shared with DVD compressed data DVD-DATA3
165	DVD-DATA4/CDGSDATA	I	DVD parallel compressed data from DVD DSP. or CD-G data indicating serial subcode data input
166	VSS	-	Connect to ground
167	VDD	-	Power supply terminal 3.3V
168	DVD-DATA5/CDG-VFSY	I	DVD parallel compressed data from DVD DSP. or CD-G frame sync indicating frame-start or composite synchronization input.
169	DVD-DATA6/CDG-SOS1	I	DVD parallel compressed data from DVD DSP. or CD-G block sync indicating block-start synchronization input

2.Pin function (5/5)

Pin No.	Symbol	I/O	Description
170	DVD-DATA7/CDG-SCLK	I	DVD parallel compressed data from DVD DSP. or CD-G clock indicating sub code data clock input or output
171	VDACK	I	In synchronous mode, bitstream data acknowledge. Asserted when DVD data is valid.Polarity is programmable
172	VREQUEST	O	Bitstream request
173	VSTROBE	I	Bitstream strobe
174	ERROR	I	Error in input data
175	VDD	-	Power supply terminal 3.3V
176	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
177	VDD	-	Power supply terminal 3.3V
178	VSS	-	Connect to ground
179	NC	-	Non connect
180	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
181	NC	-	Non connect
182	HADDR0	I	Host addressbus. 3-bit address bus selects one of eight host interface registers
183	HADDR1	I	Host addressbus. 3-bit address bus selects one of eight host interface registers
184	HADDR2	I	Host addressbus. 3-bit address bus selects one of eight host interface registers
185	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
186	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
187	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
188	VSS	-	Connect to ground
189	VDD	-	Power supply terminal 2.5V
190	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
191	VSS	-	Connect to ground
192	VDD	-	Power supply terminal 3.3V
193	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
194	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
195	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
196	RESERVED	I	Tie to VSS or VDD_3.3 as specified in table 1
197	HDATA7	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
198	VSS	-	Connect to ground
199	HDATA6	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
200	HDATA5	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
201	HDATA4	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
202	HDATA3	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
203	HDATA2	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
204	VDD	-	Power supply terminal 3.3V
205	VSS	-	Connect to ground
206	HDATA1	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
207	HDATA0	I/O	The 8-bit bi-derectional host data through which the host writes data to the decoder code.
208	CS	I	Host chip select input

■ MN101C12G (IC701) : System micom

1.Terminal layout



2.Pin function

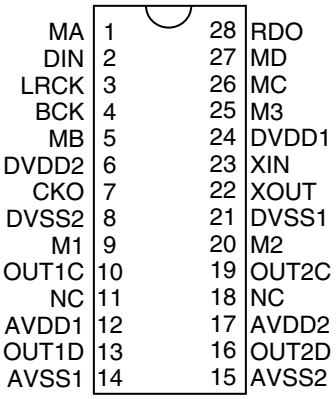
Pin No.	Symbol	I/O	Function
1	GND	-	GND
2	CS0	I	A set bit0 (It is effective in the U.E version)
3	CS1	I	A set bit1 (It is effective in the U.E version)
4	CS2	I	A set bit2 (It is effective in the U.E version)
5	NTSEL	I	NTSC/PAL switch SW input
6	POWER SW	I	Power key input
7	SHUT1	I	JOG shuttle input (AD)
8	KEY1-5	I	10 Key input (1~5)
9	KEY6-10	I	10 Key input (6~10, +10)
10	VREF	-	+B (Apply 5V)
11	VDD	-	+B (Apply 5V)
12	OSC2	O	10MHz OSC
13	OSC1	I	10MHz OSC
14	VSS	-	GND
15	-	I	Unused, Connects with GND
16	-	O	Unused
17	MMOD	I	Connects with GND
18	OSDCS3	O	V.ENCODER chip selection
19	RSTE	O	V.ENCODER reset
20	OSDDO	O	V.ENCODER communication DATA
21	S2UDT	O	Communication between unit microcomputers DATA OUT
22	U2SDT	I	Communication between unit microcomputers DATA IN
23	SCLK	O	Communication between unit microcomputers CLK
24	BUSY	O	Communication between unit microcomputers BUSY
25	CPURST	O	Unit microcomputer reset
26	REQ	I	Communication between unit microcomputers REQ
27	REMO	I	Remote control interruption
28	CS3	I	Set password change judgment bit(H:Change, L:Usual)
29	TEST	I	Un used
30	TEST	I	H:Checkers mode, L:Normal mode
31	TEST	I	H:Running mode, L:Normal mode
32	NC	I	Un used
33	RESET	I	Reset input
34	NC	O	Un uesd
35	NC	O	Un used
36	VDD	-	Un used
37	OSDCK	O	V.ENCODER communication CK
38	NT	O	NTSC/PAL Switching

MN101C12G (2/2)

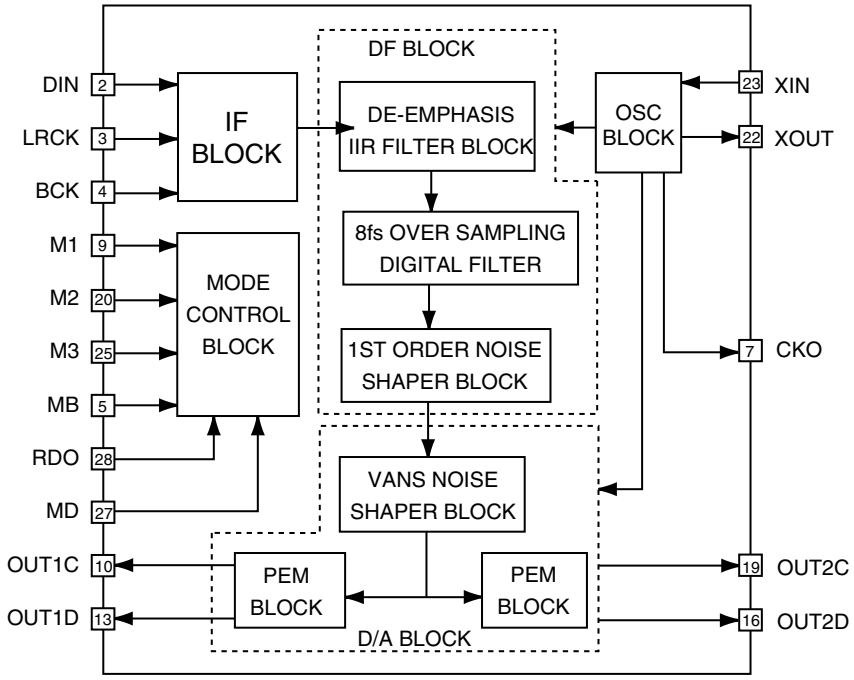
Pin No.	Symbol	I/O	Function
39	FS2	O	48kHz, 96kHz switch
40	CHREQ	I	Changer communication REQUEST
41	CHST	O	Changer communication STROBE
42	CHDATA	O	Changer communication DATAI/O
43	NC	-	Un used
44	CHCK	O	Changer communication CLOCK
45	FLDATAO	O	FL driver communication DATAO
46	FLDATAI	I	FL driver communication DATAI
47	FLCK	O	FL driver communication CLOCK
48	FLCS	O	FL driver communication CS
49	FLRST	O	FL reset output
50	EEDO	O	EEPROM communication DATAO
51	EEDI	I	EEPROM communication DATAI
52	EECK	O	EEPROM communication CLOCK
53	EECS	O	EEPROM communication CS
54	VS1	O	S1 control
55	VS3	O	S3 control(STBY:H, P.ON:L)
56	DMUT1	-	Un used
57	DMUT2	-	Un used
58	PDB2	-	Un used
59	PDB1	-	Un used
60	DEMP2	-	Un used
61	DEMP1	-	Un used
62	DENA	-	Un used
63	KARAOKE	O	KARAOKE gain control(At KARAOKE : H)
64	POWERON	O	Power ON output
65	VS2	O	S2 control
66~76	NC	O	Un used
77	AVCI	I	AV COMPULINK input
78	AVCO	O	AV COMPULINK output
79	NC	O	Un used
80	STANBYIND	O	Standby LED output
81~85	NC	O	Un used
86	CS4	O	Un used
87	MA	O	DAC control MA
88	MB	O	DAC control MB
89	M1M3	O	DAC control M1M3
90	MD	O	DAC control MD
91	MC	O	DAC control MC
92	GAIN2	-	Un used
93	GAIN1	-	Un used
94	HPMUT	O	Un used
95	DAVSS	-	Un used
96	LMUTE	O	Un used
97	CMUTE	O	Un used
98	SMUTE	O	Un used
99	MUTE	O	Front mute output
100	DAVDD	-	Apply 5V

■ MN35503-X (IC703) : D/A CONVERTER

1.Terminal layout



2.Block diagrams

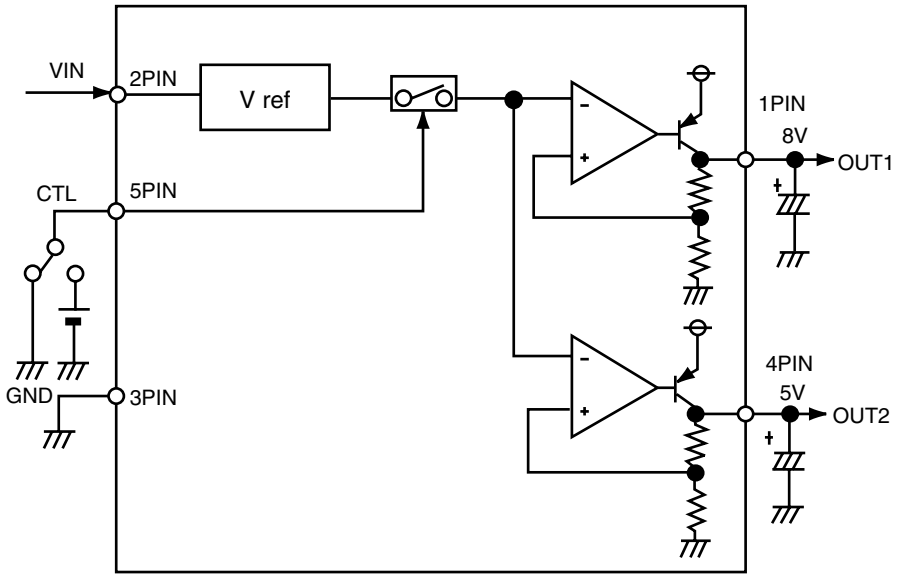


3.Pin function

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	MA	-	Connected to ground	15	AVSS2	-	Analog ground 2
2	DIN	I	Data input	16	OUT2D	O	2D PEM output
3	LRCK	I	L/R clock input	17	AVDD2	-	Analog power supply 2
4	BCK	I	Bit clock input	18	NC	-	Non connection
5	MB	I	De-emphasis ON signal	19	OUT2C	O	2C PEM output
6	DVDD2	-	Digital power supply2	20	M2	-	Connected to ground
7	CKO	I	Clock output	21	DVSS1	-	Digital ground 1
8	DVSS2	-	Digital ground 2	22	XOUT	O	Crystal oscillator output
9	M1	-	Connected to ground	23	XIN	I	Crystal oscillator input
10	OUT1C	O	1C PEM output	24	DVDD1	-	Digital power supply 1
11	NC	-	Non connect	25	M3	-	Connected to ground
12	AVDD1	-	Analog power supply 1	26	MC	-	Connected to ground
13	OUT1D	O	1D PEM output	27	MD	I	Reset signal/Digital Att.control signal input
14	AVSS1	-	Analog ground 1	28	RDO	-	Not used

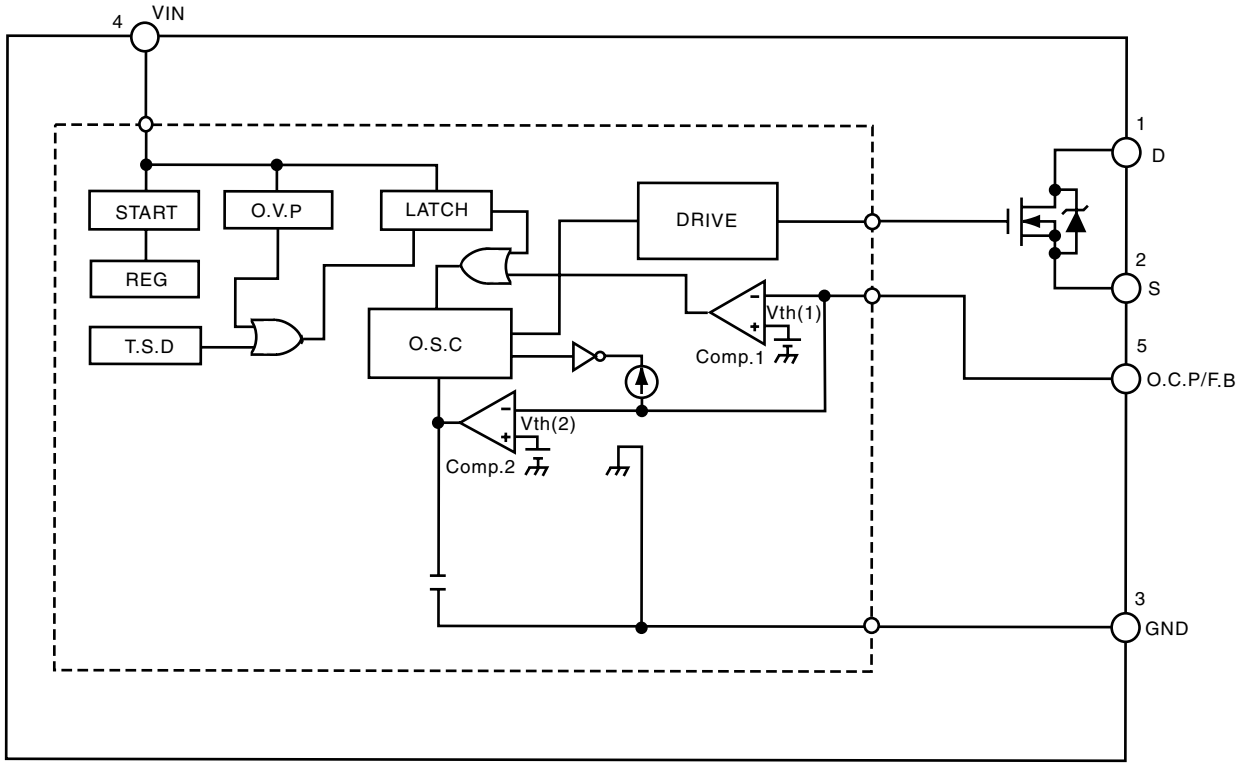
■ BA41W12ST-V5 (IC711) : Regulator

1.Block diagrams



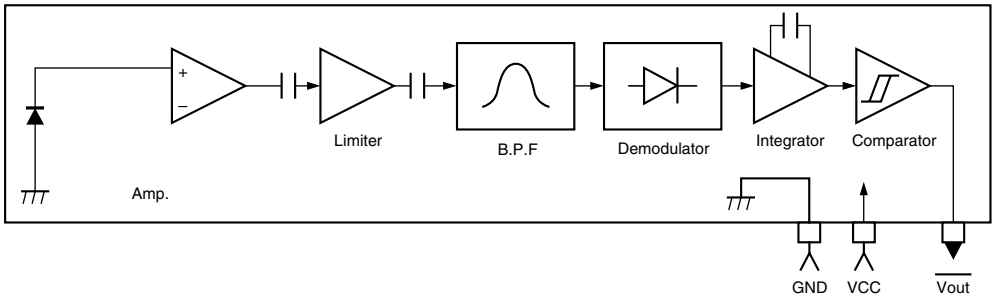
■ STR-G6651 (IC901) : Switch regulator

1.Block diagrams



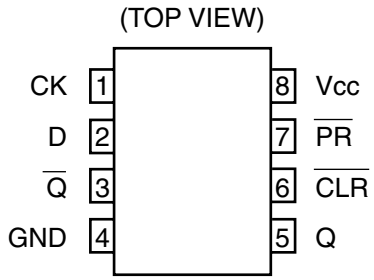
■ GP1U271X (IC801) : Receiver for remote controller

1.Block diagram

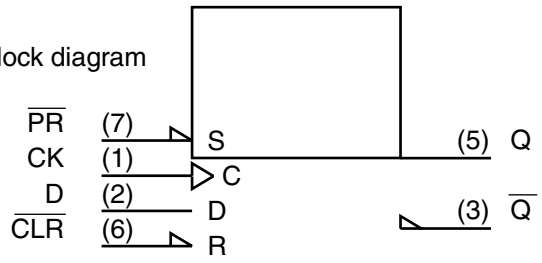


■ TC7WH74FU-X (IC321) : Clock buffer

1.Terminal layout

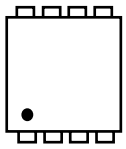


2.Block diagram

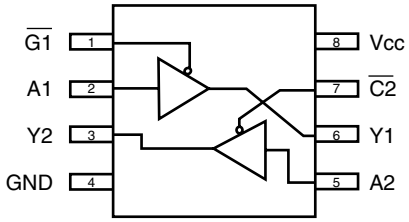


■ TC7W125FU-X (IC412) : Buffer

1. Terminal layout

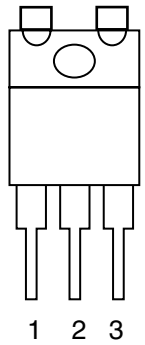


2. Block diagram



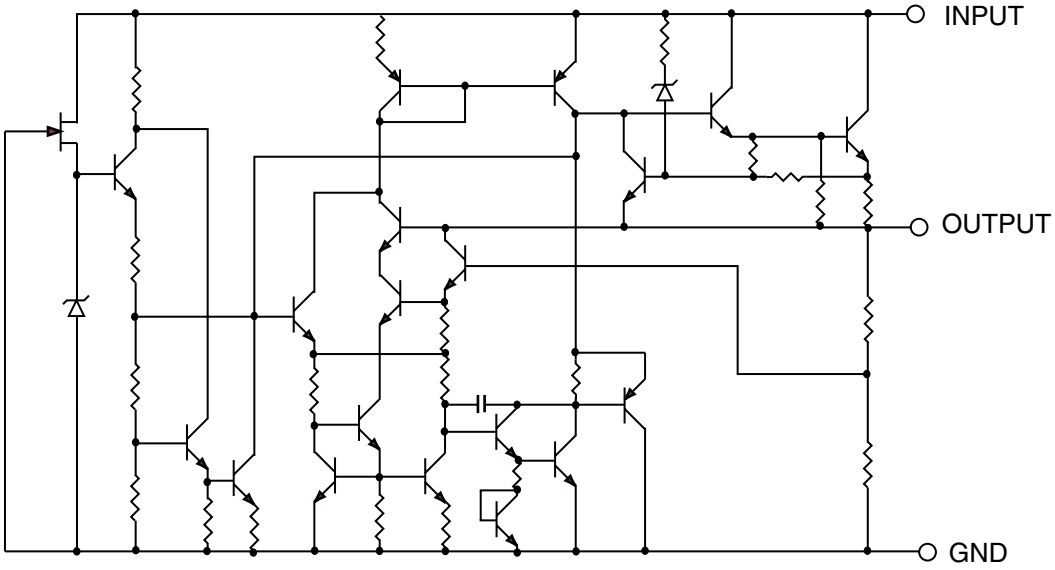
■ NJM78M05FA (IC953) : Regulator

1.Terminal layout



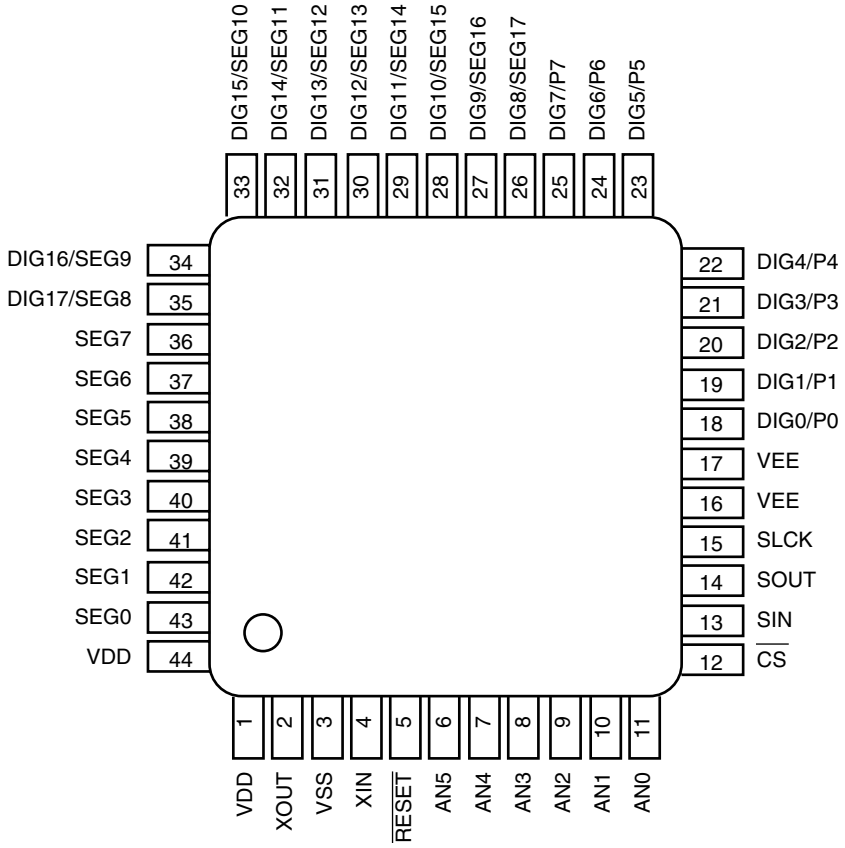
1.INPUT
2.GND
3.OUTPUT

2.Block diagram



■ M35500BGP (IC802) : FL Driver

1.Terminal layout



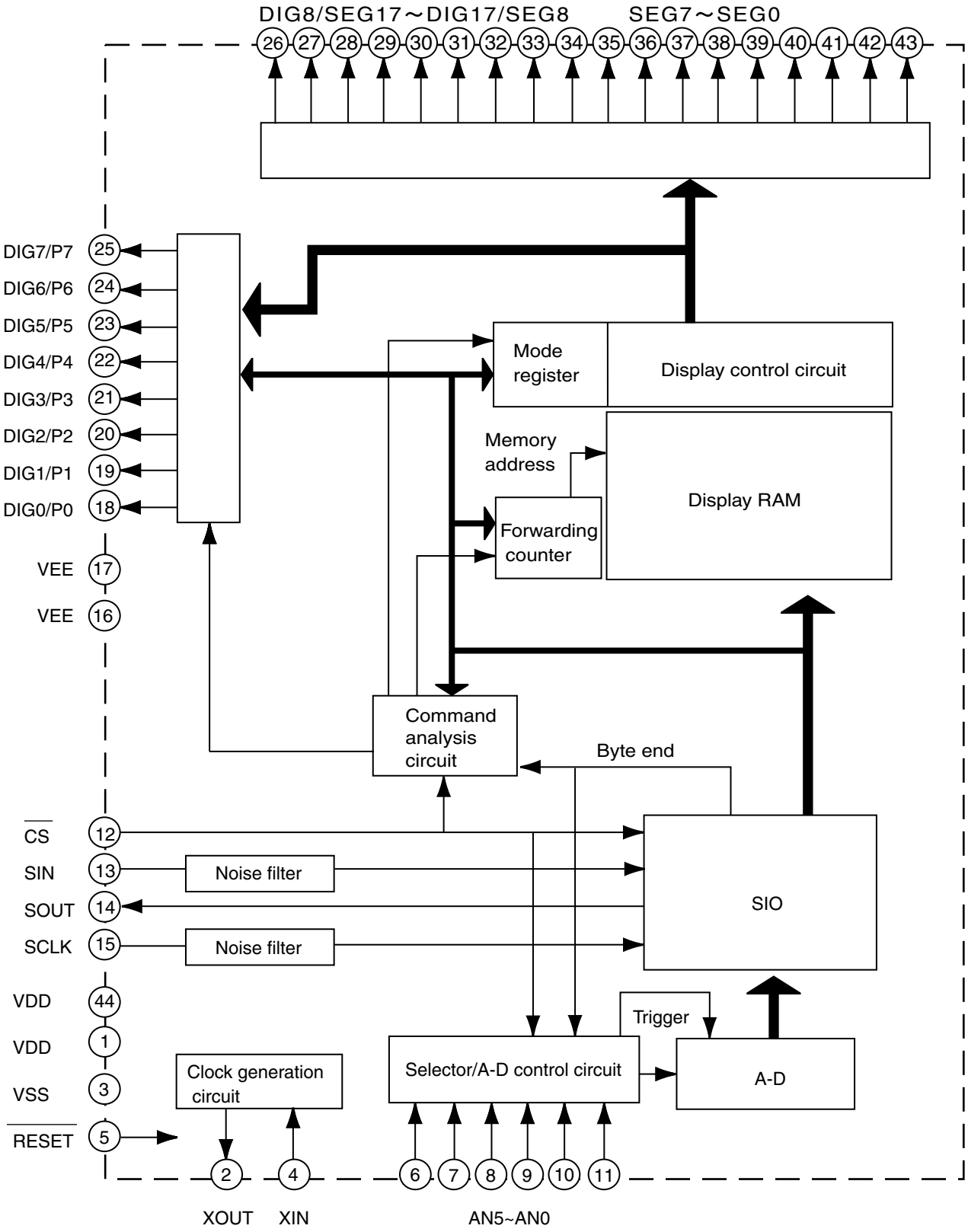
2.Pin function

M35500BGP

Pin No.	Symbol	I/O	Function
1	VDD	-	+B
2	XOUT	O	Both terminals are short-circuited on the outside, and capacity is connected.
3	VSS	-	0v is supplied to vss.
4	XIN	I	Both terminals are short-circuited on the outside, and capacity is connected.
5	$\overline{\text{RESET}}$	I	Reset input of active "L" The pull-up resistor is built into between Vcc terminals.
6	AN5	I	Key S811~S815 input
7	AN4	-	GND
8	AN3	-	GND
9	AN2	I	Key S821~S826 input
10	AN1	I	SHUTTLE control
11	AN0	I	Key S831~S836 input
12	$\overline{\text{CS}}$	I	When "L" is input, serial data can be forwarded.
13	SIN	I	The serial data is input. Take in twice continuously with the sample clock of 2MHz.
14	SOUT	O	The serial data is output. Becomes "Hiz" while resetting
15	SCLK	I	Clock of serial transfer is input.Take in twice continuously with the sample clock of 2MHz.
16	VEE	-	The voltage supplied to the pull down resistance is added.
17	VEE		
18	DIG0/P0	O	Digit output or general-purpose output terminal. At reset:Becomes "V_{EE}" level through the pull down resistance.
19	DIG1/P1		
20	DIG2/P2		
21	DIG3/P3		
22	DIG4/P4		
23	DIG5/P5		
24	DIG6/P6		
25	DIG7/P7		
26	DIG8/SEG17	O	Digit output or segment output terminal. At reset : Becomes "V_{EE}" level through the pull down resistance.
27	DIG9/SEG16		
28	DIG10/SEG15		
29	DIG11/SEG14		
30	DIG12/SEG13		
31	DIG13/SEG12		
32	DIG14/SEG11		
33	DIG15/SEG10		
34	DIG16/SEG9		
35	DIG17/SEG8		
36	SEG7	O	Segment output terminal. At reset : Becomes "V_{EE}" level through the pull down resistance.
37	SEG6		
38	SEG5		
39	SEG4		
40	SEG3		
41	SEG2		
42	SEG1		
43	SEG0		
44	VDD	-	+B

3. Block diagram

M35500BGP



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